SINGLE OFCC BASED CONTINUOUS TIME FILTER

By

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ABSTRACT

A single Operational Floating Current Conveyor (OFCC) based continuous time filter is proposed in this paper. The proposed filter can be configured for low pass, band pass and high pass responses by choosing proper impedances. It shows orthogonal controllability of pole frequency and quality factor. It can provide low pass, high pass and band pass responses by appropriately selecting component values. The verification of the theoretical proposition is done through AC and transient analysis in SPICE. The resilience of the circuit has been tested by the use of Monte Carlo analysis in SPICE.

Keywords: Continuous Time Filter, Operatonal Floating Current Conveyor, Low Pass Filters, High Pass Filters, Band Pass Filters.

INTRODUCTION

Continuous Time (CT) filters find wide applications pertaining to electronic systems namely radar, consumer electronics, instrumentation and military ordnance (Su, 2003). The design of CT filters using current mode (CM) building blocks has received considerable interest in past few years due to inherent expedients such as larger bandwidth at higher gains. The Operational Floating Current Conveyor (OFCC) (Ghallab, Badawy, Kaler & Maundy, 2005), a CM active block, is a versatile block in the sense that it has both low and high impedance terminals which facilitates processing of voltage and current signals. Variety of OFCC based circuits such as wheatstone bridge (Ghallab & Badawy, 2006), instrumentation amplifier (Ghallab et al., 2005), readout circuits (Ghallab & Badawy, 2004), rectifier (Pandey, Pandey, Nand& Kumar, 2014), logarithmic amplifier (Pandey, Tripathi, Pandey & Batra, 2014), variable gain amplifier (Hassan & Soliman, 2005), and filters (Ghallab, Badawy, Kaler, Elela & Elsaid, 2002; Ghallab, Elela & Elsaid, 2002; Ghallab, Badawy, Elela & Elsaid 2006; Pandey, Nand & Khan, 2013; Pandey, Nand & Khan, 2014) have been developed in recent past.

This paper addresses the single active block based CT filter which is particularly useful where the power and area constraints are critical. First and second order filter sections are cascaded to obtain higher order filter design to meet desired specifications. In such situation, a multiple active blocks based second order filter will not only lead to a larger silicon area but also higher power consumption as compared to single active block based design.

The objective of the paper is to develop a continuous time filter with moderate component spread, orthogonal tunability, and independent adjustment of angular frequency and gain. The study on OFCC based CT filters (Ghallab et al., 2000; Ghallab et al., 2002; Ghallab et al., 2006; Pandey et al., 2013; Pandey et al., 2014) shows that no single OFCC based filter is available in literature. Therefore, single OFCC based CT filter is proposed in this paper to bridge this gap.

This paper contains five sections including the introductory one. The port relationships of OFCC are given in Section 2 followed by presentation and detailed discussion of the proposed filter. The deviation of the proposed filter behaviour in presence of non-ideality is analysed in Section 3. SPICE simulations in both frequency and time domain are included in Section 4 to verify theoretical proposition. The paper is concluded in Section 5.

1. The Proposed Circuit

The circuit block diagram of OFCC is depicted in Figure 1.

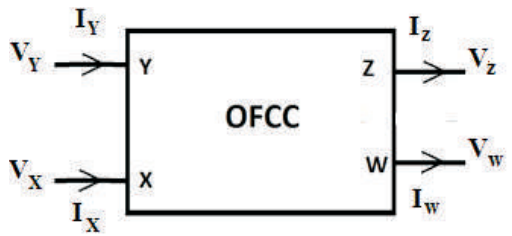

Figure 1. Circuit block of OFCC

It has two inputs (X, Y) and two outputs (W, Z) terminals. The port X has low impedance, and so it is suitable to input current while the port labeled Y presents high input impedance making it ideal for voltage input. The port Z is a high impedance current output. The terminal marked W is the low impedance output voltage.

The transmission properties of the OFCC are given by the matrix in (1):

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_Z \end{bmatrix} \quad (1)$$

Where I_j and V_j respectively represent current and voltages of j^{th} terminal (j = Y, X, W, Z). Figure 2 depicts proposed filter topology that consists of a single OFCC block along with seven other passive components. The circuit consists of two voltage dividers Z_1 and Z_4, cascaded with Z_3 and Z_5. But instead as an improvement Z_4 is bootstrapped (IEEE 100, 2000) to the output of the amplifier thereby greatly increasing the input impedance of the amplifier and helping control the operating point of the OFCC. Thus, the positive feedback helps improve the Q of the filter and the feedback through Z_6 and Z_7, and provide the gain K.

Routine analysis of the circuit of Figure 2 yields in the following transfer function

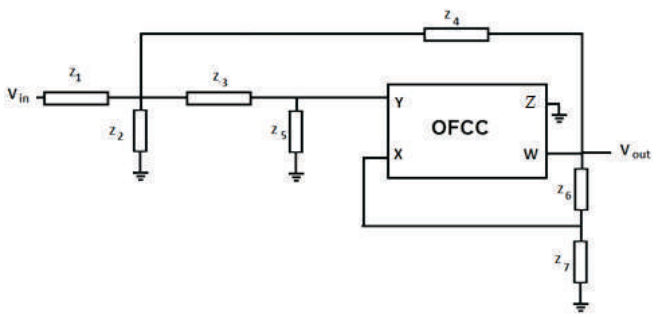

Figure 2. Proposed OFCC Filter

$$\frac{V_{out}}{V_{in}} = \frac{Z_2 Z_3 Z_4 Z_5 K}{D} \quad (2)$$

Where

$$D = Z_1 Z_5 (Z_2 Z_3 + Z_2 Z_4 + Z_3 Z_4) + Z_3^2 (Z_2 Z_4 + Z_1 Z_2 + Z_1 Z_4) + Z_2 Z_4 (Z_1 Z_3 - Z_1 Z_5 + Z_3 Z_5) - K Z_1 Z_2 Z_3 Z_5 \quad (3)$$

$$K = 1 + \frac{Z_6}{Z_7} \quad (4)$$

By choosing appropriate impedances in (2), as listed in Table 1, low pass, high pass and band pass frequency responses may be obtained.

With the impedance choices list in Table 1, the transfer function for the low pass filter is given as

$$\left.\frac{V_{out}}{V_{in}}\right|_{LP} = \frac{K/(R_1 R_3 C_1 C_2)}{s^2 + (\frac{1}{R_3 C_2} + \frac{1}{R_1 C_1} + \frac{1}{R_3 C_1} - \frac{K}{R_3 C_2})s + \frac{1}{R_1 R_3 C_1 C_2}} \quad (5)$$

The pole frequency (ω_{0_LP}), the quality factor (Q_{0_LP}), and filter gain (H_{0_LP}) are computed as:

$$\omega_{0\_LP} = \sqrt{\frac{1}{R_1 R_3 C_1 C_2}} \quad (6)$$

$$Q_{0\_LP} = \frac{\sqrt{R_1 R_3 C_1 C_2}}{R_1 C_1 + R_3 C_2 + R_3 C_2 - K R_1 C_1} \quad (7)$$

$$H_{0\_LP} = K = 1 + \frac{R_6}{R_7} \quad (8)$$

By choosing impedances corresponding to high pass response, the transfer function of (2) becomes,

$$\left.\frac{V_{out}}{V_{in}}\right|_{HP} = \frac{K s^2}{s^2 + (\frac{1}{R_4 C_1} + \frac{1}{R_5 C_2} + \frac{1}{R_5 C_1} - \frac{K}{R_4 C_1})s + \frac{1}{R_4 R_5 C_1 C_2}} \quad (9)$$

The pole frequency (ω_{0_HP}), the quality factor (Q_{0_HP}), and filter gain (H_{0_HP}) are computed as:

$$\omega_{0\_HP} = \sqrt{\frac{1}{R_4 R_5 C_1 C_2}} \quad (10)$$

$$Q_{0\_HP} = \frac{\sqrt{R_4 R_5 C_1 C_2}}{R_5 C_2 + R_4 C_1 + R_4 C_2 - K R_5 C_2} \quad (11)$$

Filter Function	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
Low Pass	R_1	∞	R_3	$1/sC_1$	$1/sC_2$	R_6	R_7
High Pass	$1/sC_1$	∞	$1/sC_2$	R_4	R_5	R_6	R_7
Band Pass	R_1	$1/sC_1$	$1/sC_2$	R_4	R_5	R_6	R_7

Table 1. Impedance Selection for Different Responses

$$H_{0\_HP} = K = 1 + \frac{R_6}{R_7} \quad (12)$$

Selecting impedances corresponding to band pass response, the transfer function of (2) modifies to,

$$\left.\frac{V_{out}}{V_{in}}\right|_{BP} = \frac{sK/(R_1C_1)}{s^2 + (\frac{1}{R_1C_1} + \frac{1}{R_5C_1} + \frac{1}{R_5C_2} + \frac{1}{R_4C_1} - \frac{K}{R_4C_1})s + \frac{R_1 + R_4}{R_1R_4R_5C_1C_2}} \quad (13)$$

The pole frequency (ω_{0_BP}), the quality factor (Q_{0_BP}), and filter gain (H_{0_BP}) are computed as:

$$\omega_{0\_BP} = \sqrt{\frac{R_1 + R_4}{R_1R_4R_5C_1C_2}} \quad (14)$$

$$Q_{0\_BP} = \frac{\sqrt{(R_1 + R_4)R_1R_4R_5C_1C_2}}{R_1R_4(C_1 + C_2) + R_4R_5C_2 + R_1R_5C_2(1 - K)} \quad (15)$$

$$H_{0\_BP} = \frac{R_4R_5C_2K}{R_1R_4(C_1 + C_2) + R_4R_5C_2 + R_1R_5C_2(1 - K)} \quad (16)$$

Considering an equicomponent design except for the impedance used to obtain gain i.e. R_6 and R_7, filter parameters such as the gain, pole frequency and quality factor of low pass, high pass and band pass responses are placed in Table 2.

It is clear from Table 2 that ω_0 can be adjusted independent of Q_0. A very high value of Q_0 can be obtained by choosing K close to 3 in case of low pass and high pass response. A K close to 4 yields a high Q_0 for the band pass response.

2. Non-Ideality Analysis

The response of the filter often deviates due to the non-ideal characteristics of the OFCC. This is due to the parasitic capacitances which causes the gain to be equal to ε times its ideal value. Considering the single pole model, the value of ε can generally be approximated as

$$\varepsilon(s) = \frac{1}{1 + sC_pR} \quad (17)$$

Filter Function	Filter Gain (H_0)	Angular Frequency (ω_0)	Quality Factor (Q_0)
Low Pass	K	$\frac{1}{RC}$	$\frac{1}{3-K}$
High Pass	K	$\frac{1}{RC}$	$\frac{1}{3-K}$
Band Pass	$\frac{K}{4-K}$	$\frac{\sqrt{2}}{RC}$	$\frac{\sqrt{2}}{4-K}$

Table 2. Filter Parameters for Equicomponent Design

Where C_p is the parasitic capacitance and R is the resistance of the feedback network. This causes the transfer function of the low pass, high pass and band pass topology to modify and become

$$\left.\frac{V_{out}}{V_{in}}\right|_{LP} = \frac{K(1/(1+sC_pR))/(R_1R_3C_1C_2)}{s^2 + (\frac{1}{R_3C_2} + \frac{1}{R_1C_1} + \frac{1}{R_3C_1} - \frac{K(1/(1+sC_pR))}{R_3C_2})s + \frac{1}{R_1R_3C_1C_2}} \quad (18)$$

$$\left.\frac{V_{out}}{V_{in}}\right|_{HP} = \frac{K(1/(1+sC_pR))s^2}{s^2 + (\frac{1}{R_4C_1} + \frac{1}{R_5C_2} + \frac{1}{R_5C_1} - \frac{K(1/(1+sC_pR))}{R_4C_1})s + \frac{1}{R_4R_5C_1C_2}} \quad (19)$$

$$\left.\frac{V_{out}}{V_{in}}\right|_{BP} = \frac{sK(1/(1+sC_pR))/(R_1C_1)}{s^2 + (\frac{1}{R_1C_1} + \frac{1}{R_5C_1} + \frac{1}{R_5C_2} + \frac{1}{R_4C_1} - \frac{K(1/(1+sC_pR))}{R_4C_1})s + \frac{R_1 + R_4}{R_1R_4R_5C_1C_2}} \quad (20)$$

The effect of an additional pole will thus be caused due to the parasitic capacitance which can be ignored by selecting the operating frequency range of this continuous time filter much lower than the parasitic pole frequency.

3. Simulation Results

The OFCC implemented using CMOS(Hassan and Soliman, 2005), as given in Figure 3 is used to verify the operation of the proposed filters. Simulation using SPICE has been done for this purpose using the aspect ratio of various transistors as given in Table 3. Supply voltages (VDD and VSS) are taken as ± 1.5V and bias voltages (VB1 and VB2) of ± 0.8V are applied.

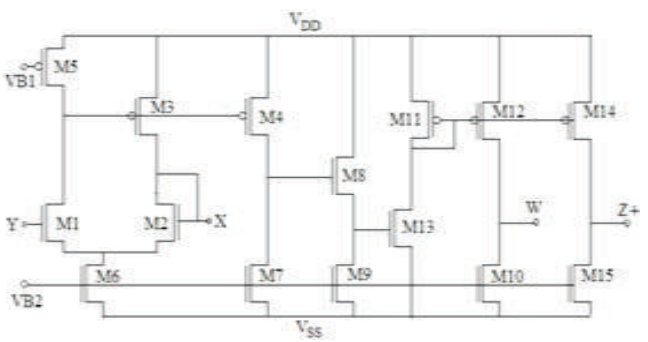

Figure 3. CMOS schematic of OFCC (Hassan and Soliman, 2005)

Transistor	W(μm) / L(μm)
M1, M2	50 / 1
M3, M4, M11, M12, M14	50 / 2.5
M5, M7, M10, M15	20 / 2.5
M6, M8	40 / 2.5
M9, M13	100 / 2.5

Table 3. Transistors aspect ratios of the circuit shown in Figure 3 (Hassan and Soliman, 2005)

To test the frequency response of the band pass configuration, the filter is designed for center frequency 2.25MHz by taking R1=R4=R5=1KΩ and C1=C2=0.1nF. The values of (R6, R7) are chosen as (1KΩ, 1KΩ), (2KΩ, 1KΩ) and (5.6KΩ, 2KΩ) for Q0=0.71, 1.41 and 7.07 respectively as presented in Figure 4. (a). The frequency response of low pass and high pass configuration for pole frequency of 1.59MHz are presented in Figure 4. (b) where all the resistors and capacitors are taken as 1KΩ and 0.1nF respectively. The low pass and high pass responses with

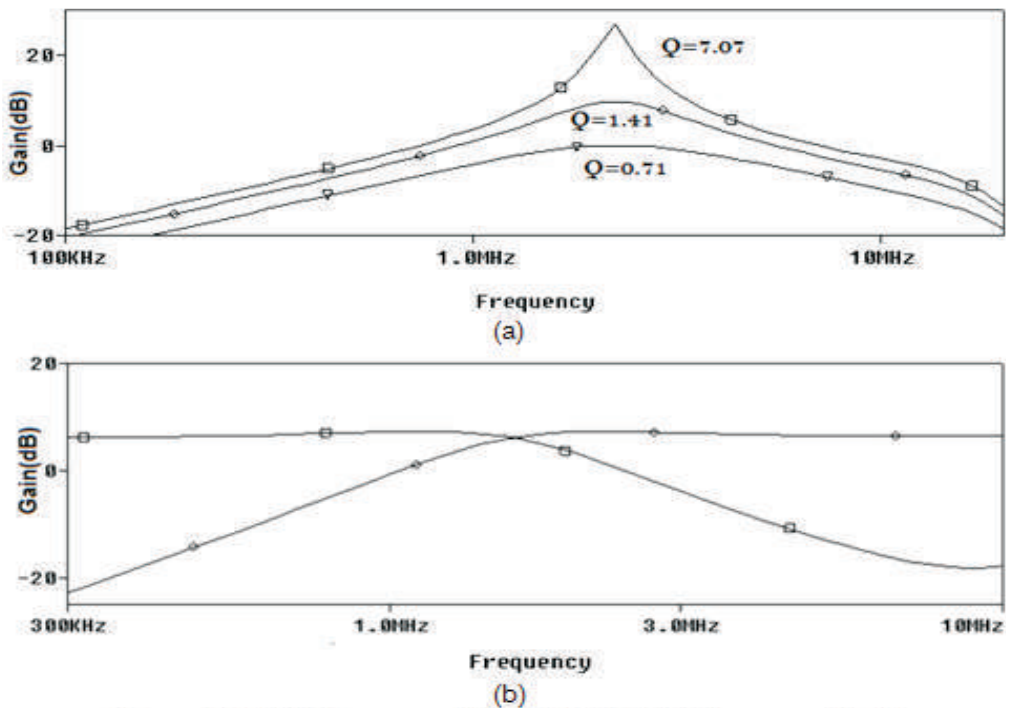

Figure 4 (a) BP Response (Gain) (b) LP & HP Response (Gain)

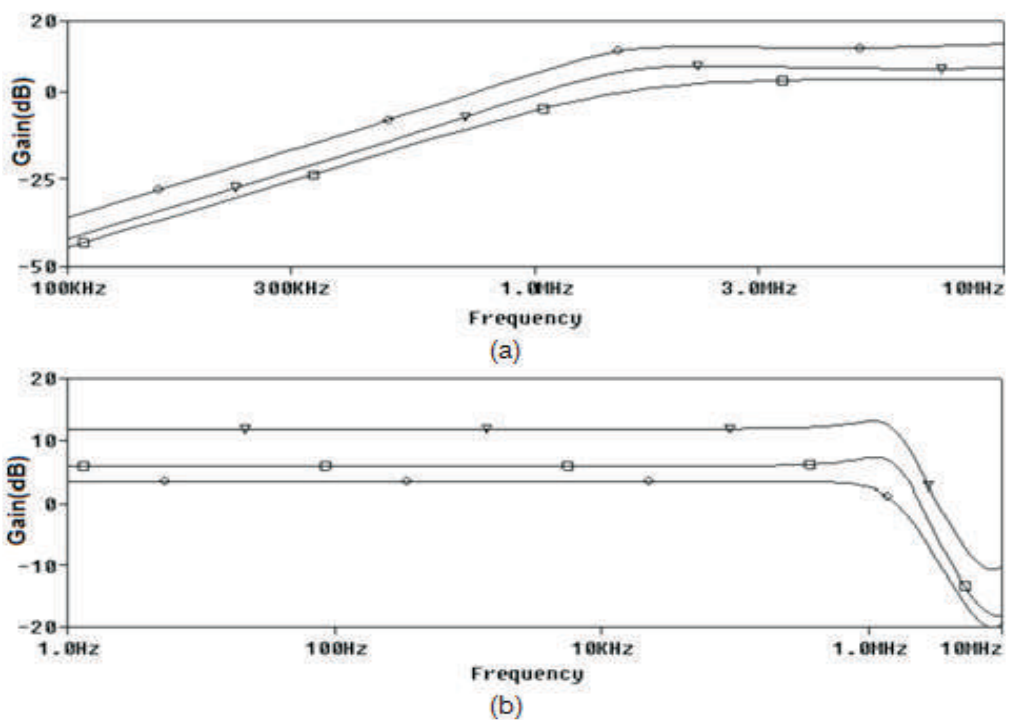

Figure 5 (a) HP Response (constant f_0 =1.59 and varying Gain (1.5, 2, 4)), (b) LP Response (constant f_0 =1.59 and varying Gain (1.5, 2, 4))

gain 1.5, 2 and 4 while keeping the pole frequency at 1.59MHz are also obtained by choosing (R6, R7) as (1KΩ, 2KΩ), (1KΩ, 1KΩ) and (3KΩ, 1KΩ) respectively. Figure 5 (a) and (b) depict plot to this context. The response to the variation in pole frequency by keeping K constant and taking R1=R4=R5=1KΩ is shown in Figure 6 for band pass filter. The values of (C1, C2) are chosen as (0.1nF, 0.1nF), (0.05nF, 0.05nF) and (0.2nF, 0.2nF) for pole frequency 2.25MHz, 4.5MHz and 1.13MHz respectively.

To investigate the time domain behavior of the proposed filter, the band pass topology with f0 =2.25MHz, Q = 0.71 and H = 1 is considered. An input signal of three sinusoids 100 KHz, 1 MHz and 10 MHz is applied. The time domain response and corresponding frequency spectrum is shown in Figure 7 and Figure 8. It is clear that amplitudes of sinusoids having frequency 100 KHz and 10 MHz are significantly deteriorated whereas the signal with 1MHz frequency passes with the minimum deterioration. Another simulation is carried out to check the phase performance of low pass response by applying a sinusoid of 1.59MHz frequency to a filter with f0=1.59MHz. The input and output time domain response are shown in

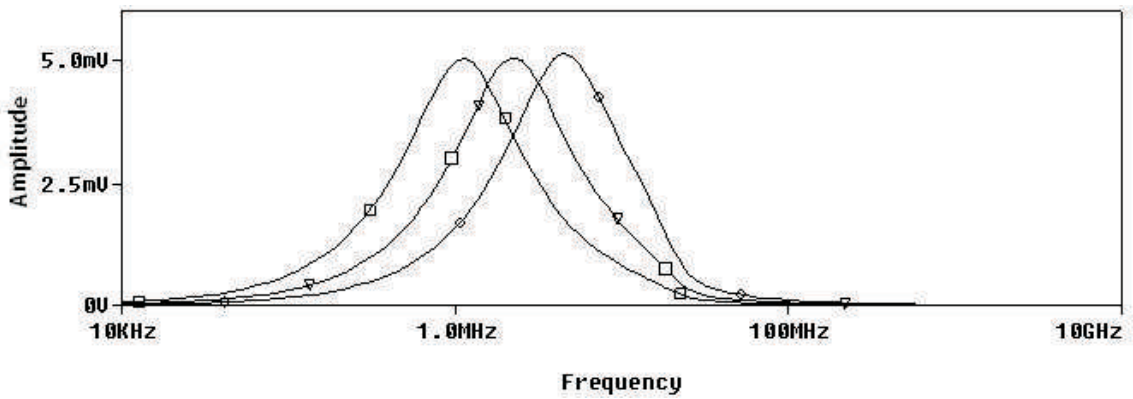

Figure 6. BP Response (f_o=2.25MHz, 4.5MHz and 1.13MHz)

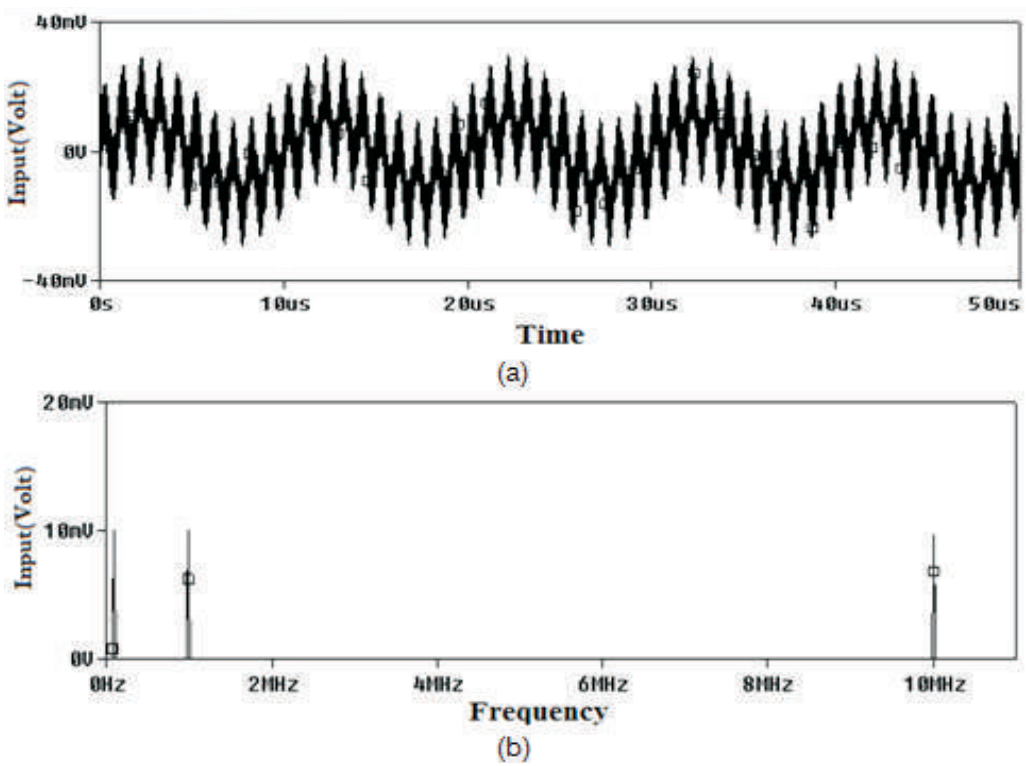

Figure 7 (a) Three source input (b) Three source input (FFT)

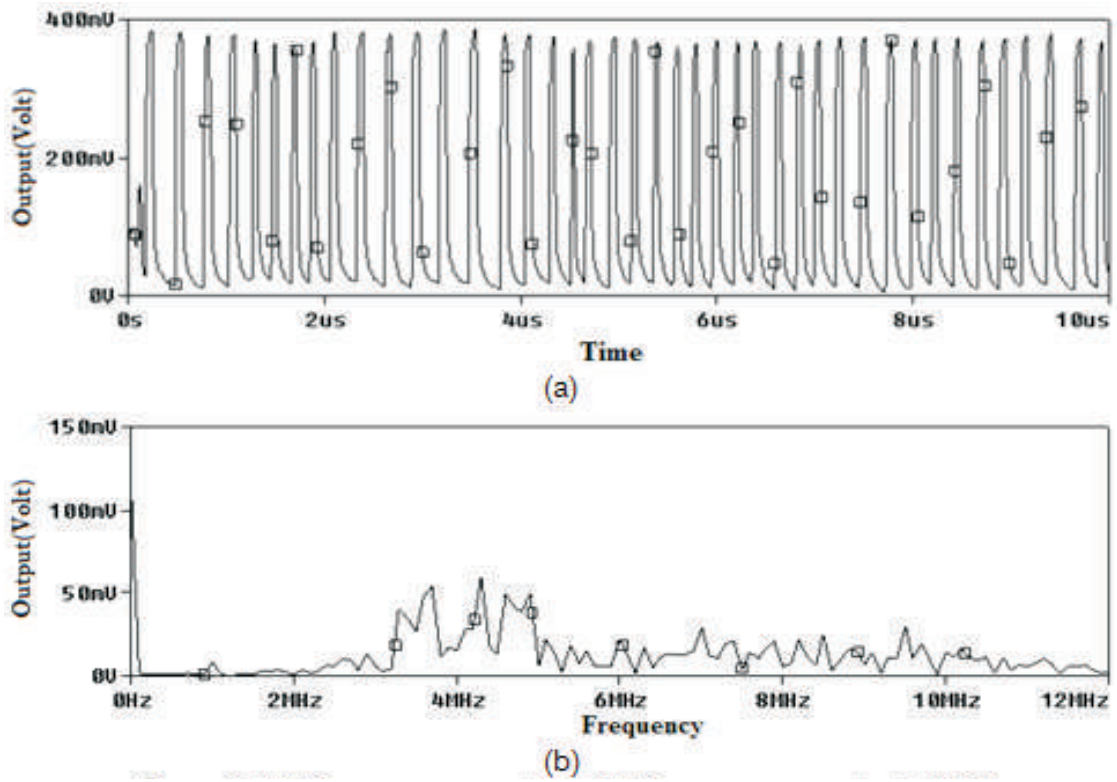

Figure 8 (a) Three source output (b) Three source output (FFT)

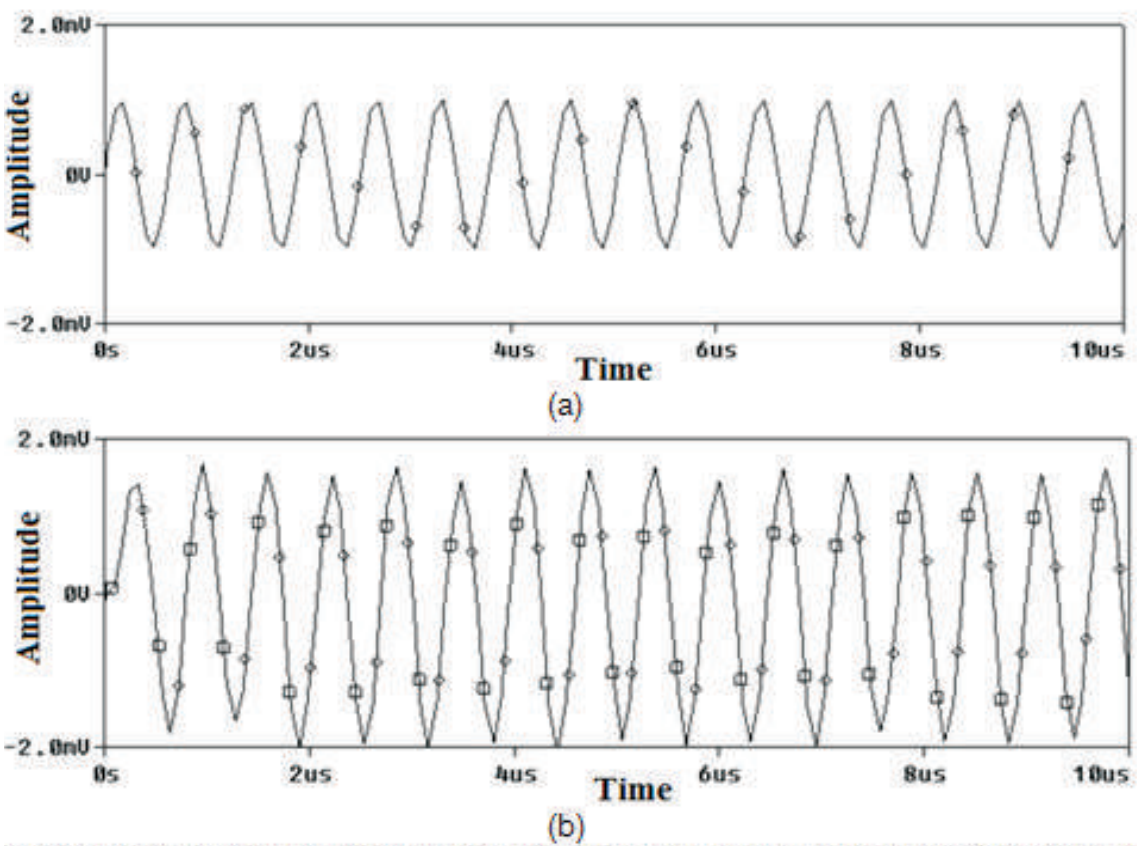

Figure 9 (a) Cut off frequency is equal to source frequency (Input) (b) Cut off frequency is equal to source frequency (Output)

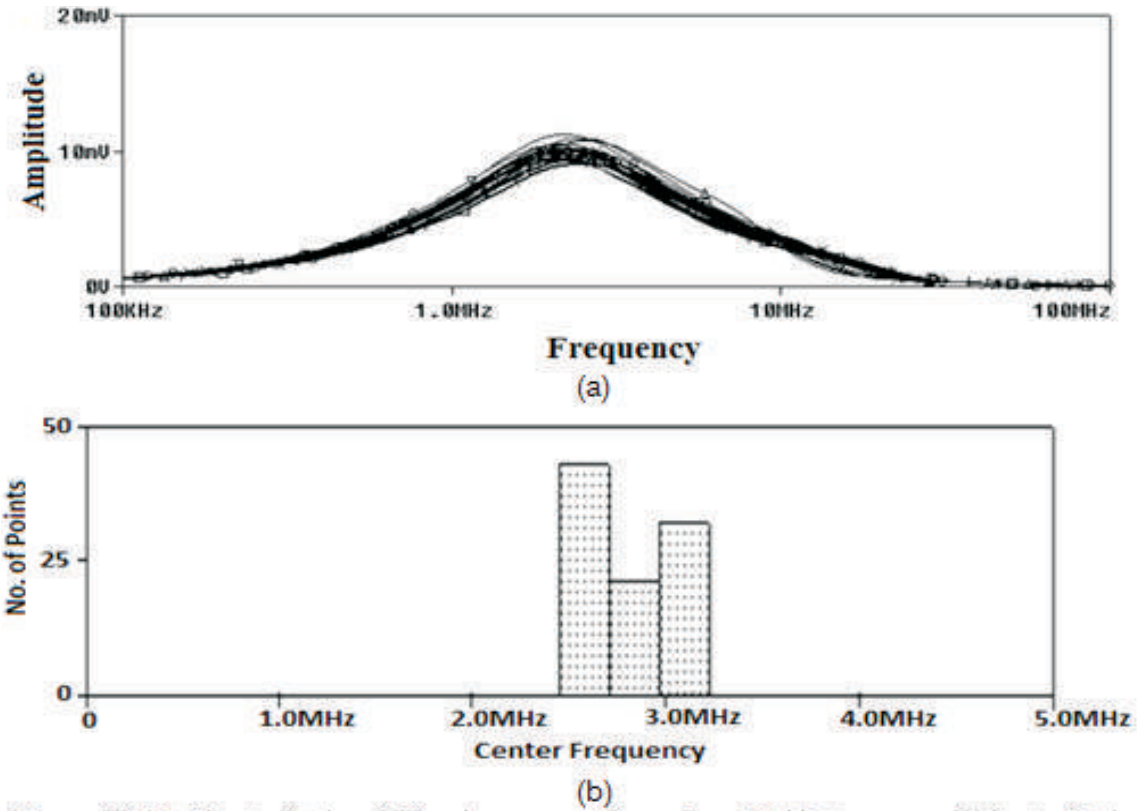

Figure 10 (a) Monte Carlo of Band pass configuration (b) Histogram of Monte Carlo

Figure 9. Monte Carlo analysis has been carried out to check the resilience of the circuit. The frequency response of the Monte Carlo analysis with component tolerance of (±5) % is shown in Figure 10.

Conclusion

In this paper, a single OFCC continuous time filter topology is proposed. It can be configured as low pass, band pass and high pass filter upon proper selection of impedance values. The pole frequency, quality factor and bandwidth are controllable using various passive components. The design is simple and the gain can be easily controlled by varying the values of the resistors. The proposed circuit has been tested using SPICE simulations. The results of the time domain, frequency domain and Monte Carlo analysis justify the resilience of the circuit.

The proposed circuit is an ideal replacement in the modern day transceivers. The circuit can work in all three configurations and possesses orthogonal tunability of filter parameters. The filter also provides variation in quality factor and gain, independent of the center frequency. Moderate component spread is required to achieve high Q factor. The filter possesses high bandwidth and shows immunity to slew related problems. It can thus be used to replace present day filters because of the above mentioned advantages.

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