APPLICATION OF RESONANT CONVERTER TO REGULATED POWER SUPPLY

By

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ABSTRACT

In this paper a pulse width modulated series parallel resonant converter is presented. The performance of the converter for constant output voltage with variable input and variable load is analyzed. This configuration is well suited for many applications where output is fairly constant but the input is required to vary widely without serious switching losses and with significant reduction in ripple content. Experimental results obtained from a laboratory prototype are presented.

Keywords: Zero Voltage Switching, Zero Current switching, DC-DC Converter, Resonant Converter, Soft Switching.

INTRODUCTION

Switch mode power conversion is one of the elegant ways of electric power processing in today's industrial environment, due to circuit simplicity, ease of control, and improved efficiency. The recent trend in switch mode conversion is to increase the power density and to reduce the size of energy storage components, which requires operation at high switching frequencies. There are fundamentally two different circuit schemes of electronic power processing technology. They are Pulse Width Modulation (PWM), and resonance. In all pulse width modulated DC to DC and DC to AC converters, the controllable switches are operated in a switch mode where they are required to turn on and turn off the entire load current during each switching in this switched mode operation, the switches are subjected to high switching stresses and high switching power losses, that increase linearly with the switching frequency of PWM[1]. Another significant draw back of switch mode operation is the EMI produced by large di/dt and dv/dt caused by switched mode operation [2].

The series parallel resonant converter is a preferred topology for dc-dc power conversion. Its main attractive features are Zero Voltage turn on Switching (ZVS), constant switching frequency and simple control similar to that of hard switched full bridge PWM converter[3]. Resonant dc-dc converters are particularly used where high switching frequency are needed to minimize reactive component size since by operating the converters above the resonant tank natural frequency, lossless switching conditions may be achieved[4]. The series parallel converter is a particularly attractive topology since it combines a wide operating range with modest component rating. Operation of resonant converter above resonance (lagging power factor mode) results in a number of advantages. They are elimination of di/dt inductors and lossy snubbers, use of slow recovery diodes internal to MOSFET's reduced size of magnetic components etc [5]. The major limitation of high peak reverse voltage developed across the devices can be overcome by incorporating anti parallel diodes across each diode. The inverse diode associated with the device is sufficient to operate the circuit at hundreds of kilohertz, which allows to a use a diode having low turn off time. The frequency of operation is chosen to obtain the desired power handling capacity [6].

1.Analysis of Series Parallel Resonant Converter

1.1. Circuit Description

The basis circuit diagram of resonant converter is shown in Figure1. S_1 - S_4 are switching devices having base turnoff capability. D_1 to D_4 are anti parallel diodes across the switching devices. This can also be the internal diode of MOSFET. If they have slow recovery characteristics, external fast recovery diodes have to be used. The MOSFET (say S_1) and its anti parallel diodes (say D_1) acts as a bidirectional switch. Ls, Cs, Cp are resonant series

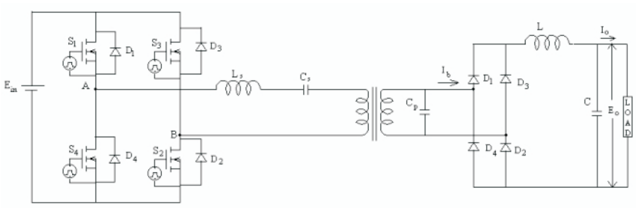


Figure1. Basic Circuit diagram of Series Parallel Resonant converter

inductor, series resonant capacitor, and parallel resonant capacitor respectively. In this circuit to make use of leakage inductance of high frequency transformer, the parallel resonant capacitor placed on the secondary of the transformer. The output voltage V_{AB} of High Frequency Inverter Bridge is applied to the tank circuit.

The diodes used in high frequency bridge rectifier should have fast recovery characteristics. LC comprises a low pass filter for smoother output voltage and current and a load is connected across the filter output.

1.2. Circuit Modeling

The load current I_0 is considered constant since a large inductor is assumed at the output circuit. Consequently the current to the input bridge rectifier I_b (t) has constant amplitude $+I_0$ or $-I_0$ depending on whether the voltage V_{cp} (t) is +ve or -ve respectively. Hence the output circuit can be represented as constant current sink qI_0, where q=+1 when V_{cp} (t) is =+ otherwise q= -1.

The switching frequency is constant and power control is obtained by phase shifting the gating signals to vary the pulse width. The converter is designed to operate from maximum to minimum pulse width. When the controllable switches are switched on in its sequence, a square wave voltage is impressed across the terminal AB. The phase angle between the gating signals is controlled to regulate the load voltage with variation with the load current or the input supply voltage. As the load current decreases to regulate output voltage the pulse width is decreased by phase shifting the gating signalsG_2 and G_4 respectively with respect to G_1 and G_3 as shown in Figure 2. It must be noted that gating signal G_1 and G_3 (also G_2 and G_4) are always 180° out of phase. The voltage across the terminals A and B, V_{AB} depends upon the switching status of the switches. When the gating signal G_1 is present then V_{AB} (t) = $+E_{in}$ if G_2 also present, otherwise=0.Similarly V_{AB} (t) = $-E_{in}$ or 0

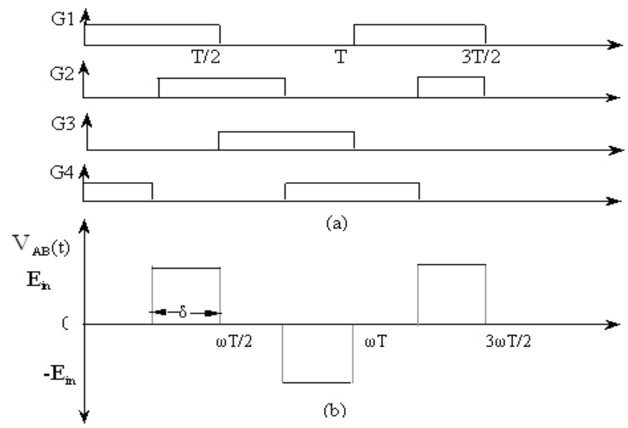


Figure 2. (a) Gating signals (b) V_{AB} (t)

depending on switching status of G_3 and G_4.

The equivalent reactance across the terminal AB may be capacitive or inductive. If it is capacitive, thyristors may be used and the converter then operates below resonant frequency. The lagging power factor mode, which occurs when the effective reactance is inductive, then the switches, is capable of gate or base turnoff may be used.

2.Modes of Series-parallel Resonant Converter

The principle of resonant converter can be explained with its different operating modes. The resonant converter can operate in five different modes. However the broad classification of modes can be made depending on the duty ratio. When the duty ratio is 1, the resonant converter can operate in two modes. The other modes are obtained when duty ratio is less than 1, depending upon the frequency of operation, circuit impedance across terminal AB and pulse width. When pulse width is maximum (Duty ratio D=1) the resonant converter can operate in two different modes.

2.1. Operation of Circuit in Mode 1

As explained the mode 1 results when the duty ratio is 1, with the condition that equivalent circuit impedance across AB is capacitive. The inductor current i (t) lead the voltage applied to the tank thus converter operates in leading power factor mode. Figure 3. shows typical Waveforms for this mode of operation. The switches S_1 & S_2 are turned on at t=0. The tank voltage becomes + E_{in} immediately. When the resonant current reaches zero at t = t_2, S_1 & S_2 are naturally commutated. Therefore zero current turn off is realized. As the resonant current reverses

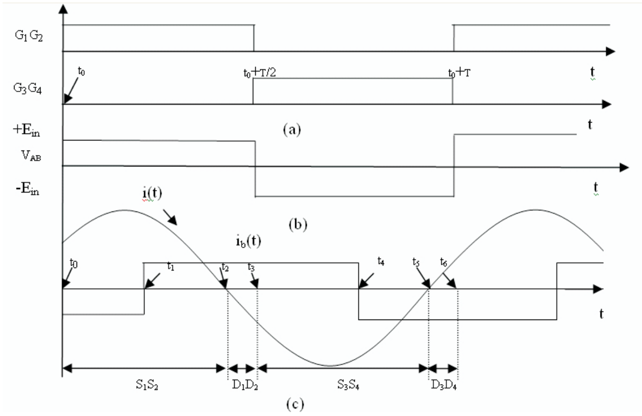


Figure 3. Typicalwaveform in mode-1
(a) GatingSignal (b) V_{AB} (t) (c) i (t) and i_b(t)

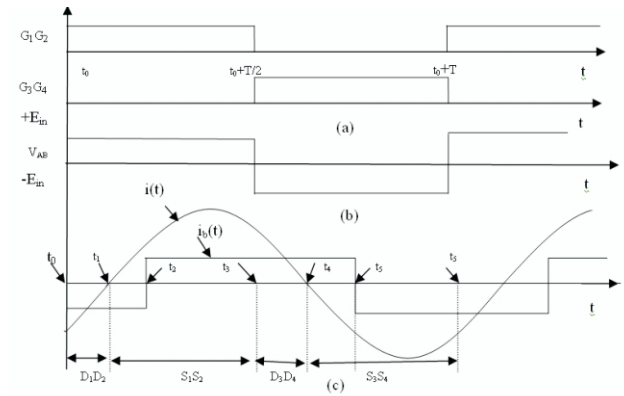


Figure 4. Typical waveform in mode - 2
(a) Gating Signal (b) V_{AB} (t) (c) i (t) and i_b(t)

at t = t_2, with the tank connected to + E_{in}, D_1 & D_2 turn on allowing a part of the tank energy to return to the source during the time interval t_2 - t_3. At the instant t = t_3, switches S_3 & S_4 are turned on and V_{AB} changes from +E_{in} to -E_{in}. At t = t_5 when i(t) becomes zero and begins to reverse forcing the diodes D_3 & D_4 to conduct. The interval t_2 - t_3 & t_5 & t_6 are called Regenerative Interval (RI) and the intervals t_0 - t_2 and t_3 -t_5 are called power intervals. Thus in this mode there are two RI & two PI.

As the switches are on at a finite current and at finite voltages, this results in turn on switching power loss. If the diodes have slow recovery characteristics, at t = t_0 large reverse current may flow through D_3 S_1 & D_4 S_2. In order to avoid these current and to minimize the diode turn off losses, the freewheeling diodes should have fast recovery characteristics. It is also evident that mode 1 requires lossy snubber & di/dt limiting inductors.

2.2. Operations of Circuit in Mode 2

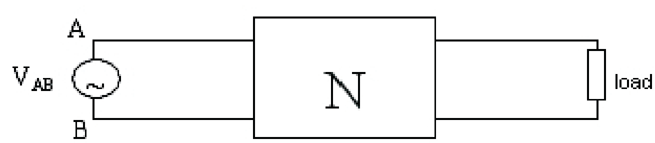
Mode 2 also occurs at duty ratio of 1. However equivalent reactance across AB is inductive. In this mode switching frequency is more than series resonant frequency and equivalent reactance is inductive across the terminal AB. The converter operates at lagging power factor (above resonance) mode. Figure 4. shows typical waveforms for this mode of operation. It is evident from the figure that diodes D_1 & D_2 are conducting initially at t = t_0.

When the current through the diode reaches zero at time t=t_1, switches S_1 & S_2 are tuned on and the currents is transferred from the anti-parallel diodes. The converter operates in the power interval till t=t_3. There is no voltage across the switches at turn on (since D_1 & D_2 are conducting) which eliminates turn on losses and facilitates operation of switches with loss less snubbers. At time t = t_3, the transition from power interval to regenerative interval takes place. At time t = t_3 i.e. (t_0 + T/2) when switches S_1 & S_2 are turned off, the current is transformed to D_3 & D_4 Turn off losses are present in such type of operation because during turn off, current and voltage are simultaneously present at the switch. The sequence of events repeats in the next half cycle. Interval t_0-t_1 & t_3-t_4 are called regenerative interval and t_1-t_3 & t_4-t_5 are power interval.

3.Mathematical Analysis of Converter

Figure 5 shows the A.C. equivalent circuit of series parallel resonant converter. The following assumptions are used in the mathematical analysis of the series - parallel resonant converter.

a. The switches, diodes, inductors, capacitors and snubber components used are ideal.
b. The effects of snubber are neglected.
c. The filter inductance is large enough to keep the load current constant.



Where N - is the resonant network
R_{ac} - AC equivalent load resistance
V_{AB} - RMS fundamental component of V_{AB}

Figure 5. A.C Equivalent Circuit of Resonant Converter

d. The high frequency transformer is ideal and has unity turns ratio.

Where N - is the resonant network

R_{ac} - AC equivalent load resistance

V_{AB} - RMS fundamental component of V_{AB}

From the output circuit of bridge rectifier and filter component to resonant converter Figure 6, V_{cp} and I_b represent the rms fundamental component of V_{cp} (t) and I_b (t) respectively. The output circuit consists of the diode bridge rectifier and inductive filter present in the output circuit.

The D.C. output voltage is obtained as the average of A.C. input voltage, Vcp

$$E_0 \quad \frac{1}{} \sqrt{2}V_{cp} \sin \quad td \quad t \qquad (1)$$

$$E_0 \quad \frac{2\sqrt{2}}{} V_{cp} \qquad (2)$$

= 2 f and f is the switching frequency.

The fundamental component of Diode Bridge current is calculated using Fourier analysis as

$$I_b \quad \frac{1}{} \int_0^{2} i_b \; t \sin \quad td \quad t \qquad (3)$$

$$I_b \quad \frac{2\sqrt{2}}{} I_0 \qquad (4)$$

Using Equation (2) & (4) the equivalent A.C. resistance as seen at the input of the rectifier bridge is given by

$$R_{ac} \quad \frac{V_{cp}}{I_b} \quad \frac{^2}{8} R_L \qquad (5)$$

and D are related by

$$= \quad D \qquad (6)$$

The duty ratio D is defined as the ratio of the time duration for which the switch S_1 & S_2 or S_3 & S_4 are switched on simultaneously i.e. t_{on} to the half of the switching period (T/2) i.e., D = t_{on}/ (T/2).When the switches S_1 and S_2 (S_3 or S_4) are switched on simultaneously, the voltage across A and B is the input voltage E_{in}.

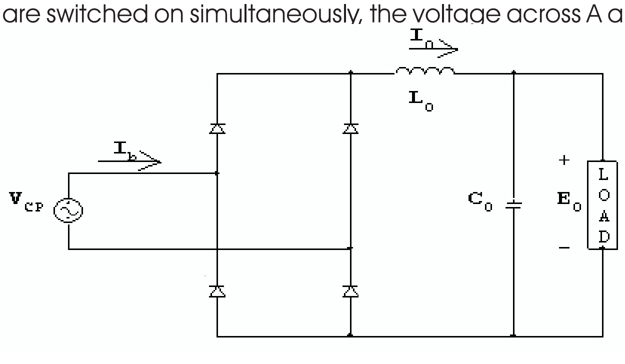


Figure 6. Output Circuit of Bridge Rectifier and filter component to resonant converter

The R.M.S. fundamental Voltage across A and B is given by

$$V_{AB} \quad \frac{1}{\sqrt{2}} \int_0^{2} V_{AB} \; t \sin \quad td \quad t \qquad (7)$$

$$V_{AB} \quad \frac{1}{\sqrt{2}} \int_{/2}^{/2} E_{in} \sin \quad td \quad t \quad \int_{3 \; /2}^{3 \; /2} E_{in} \sin \quad td \quad t \qquad (8)$$

$$V_{AB} \quad \frac{2\sqrt{2}E_{in} \sin \quad /2}{} \qquad (9)$$

Its equivalent circuit shown in Figure 8 replaces the equivalent circuit of the converter across the terminal A and B shown in Figure 5. In order to simplify the presentation, all the equations are normalized using the following base quantities.

Base voltage = E_{in}

Base impedance = $_0$L

Base current = E_{in}/ $_0$L

Base frequency $_0$ = 1/√LC

The RMS fundamental voltage across the parallel capacitor C_p is given by

$$V_{cp} \quad \frac{V_{AB}}{j \; X_L \quad X_{cs} \quad \frac{1}{\frac{1}{R_{ac}} \quad \frac{1}{jX_{cp}}}} \quad \frac{1}{\frac{1}{R_{ac}} \quad \frac{1}{jX_{cp}}} \qquad (10)$$

Here

X_L = L, X_{cs} = 1/ C_s , X_{cp} = 1/ C_p (11)

Substituting the eqn (11) in eqn (10), the equation becomes

$$V_{cp} \quad \frac{V_{AB}}{1 \quad \frac{C_P}{C_S} \quad {}^2 LC_P \quad j\frac{8}{^2}} \quad \frac{L}{R_L} \quad \frac{1}{C_S R_L} \qquad (12)$$

Substituting the eqn (9) in eqn (12) and after simplification, the equation becomes

$$V_{cp} \quad \frac{2\sqrt{2}E_{in} \sin \quad /2}{\frac{m \quad 1}{m} \quad 1 \quad y^2 \quad \frac{8}{^2} jQ \quad y \quad \frac{1}{(m \quad 1)y}} \qquad (13)$$

where

m = C_s/ C_p , Q = $_o$L/R_L = 1/ $_o$CR_L , y = / $_o$ (14)

Substituting eqn (13) in eqn (2) and after normalization , the equation(15) becomes

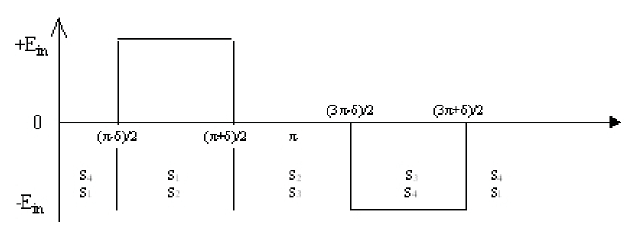


Figure 7. Quasi - Square Voltage Waveform of Resonant Converter

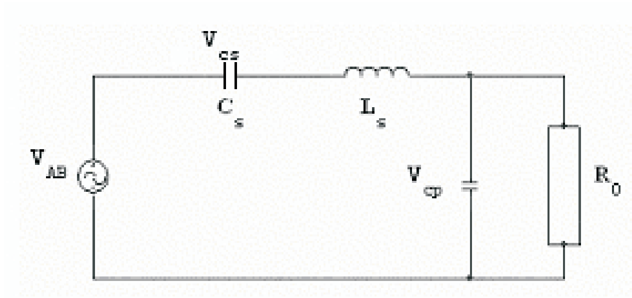


Figure 8. AC Equivalent Circuit of Resonant Converter

$$\frac{E_0}{E_i} \quad \frac{\sin \quad /2}{\frac{2}{8} \frac{m \quad 1}{m} \quad 1 \quad y^2 \qquad jQ \quad y \qquad \frac{1}{m \quad 1 \, y}} \quad (15)$$

The equivalent impedance across the terminals A and B is given by

$$Z_{eq} \quad j \; X_L \quad X_{CS} \qquad \frac{1}{\frac{1}{R_{ac}} \quad \frac{1}{jX_{CP}}} \quad (16)$$

Substituting eqn(5), eqn(11) in eqn(14), the equation becomes

$$Z_{eq} \quad j \; \frac{L}{R_L} \quad \frac{1}{C_S R_L} \qquad \frac{1}{\frac{8}{2} \quad j \; C_P R_L} \quad (17)$$

Using eqn(11) in eqn(17) and after simplification, the equation becomes

$$Z_{eq} \quad jR_L Q \; y \quad \frac{1}{m \quad 1 \, y} \qquad \frac{1}{\frac{8}{2} \quad j\frac{y \; m \quad 1}{Qm}} \quad (18)$$

After simplification and rearranging the terms we get

$$Z_{eq} \qquad {}_0 L \frac{B_1 \quad jB_2}{B_3} \quad (19)$$

Where

$$B_1 \quad \frac{8Q}{2} \quad \frac{m}{y \; m \quad 1}^{\;2} \quad (20)$$

$$B_2 \quad y \qquad \frac{1}{y \; m \quad 1} \quad B_3 \qquad \frac{m}{y(m \quad 1)} \quad (21)$$

$$B_3 \quad 1 \qquad \frac{8Qm}{{}^2 y(m \quad 1)} \quad (22)$$

Normalizing eqn (19), the equation becomes

$$Z_{eqpu} \qquad \frac{B_1 \quad jB_2}{B_3} \qquad |Z_{eqpu}| e^{j} \quad (23)$$

$$|Z_{eqpu}| \qquad \frac{\sqrt{B_1^2 \quad B_2^2}}{B_3^2} \quad (24)$$

Impedance angle $\tan^{\;1} \frac{B_1}{B_2}$ (25)

The resonant link current I

$$I \quad \frac{V_{AB}}{Z_{equ}} \quad (26)$$

$$I \qquad |I| \quad (27)$$

where

$$|I| \qquad \frac{V_{AB}}{|Z_{equ}|} \quad (28)$$

Substituting eqn (9) in eqn (4) and after normalization, the equation becomes

$$|I|_{pu} \qquad \frac{2\sqrt{2} \sin \frac{}{2}}{|Z_{equ}|} \quad (29)$$

Peak Inductor is given by

$$|I|_{ppu} \quad \sqrt{2}|I|_{ppu} \qquad \frac{4 \sin \frac{}{2}}{|Z_{equ}|} \quad (30)$$

$$|V_{cs}|_{ppu} \qquad |I| \frac{X_{cs}}{{}_0 L} \quad (31)$$

Using (30) Peak Voltage across C_s is calculated as

$$|V_{cs}|_{ppu} \qquad \frac{|I|_{ppu}}{y(m \quad 1)} \quad (32)$$

The peak Voltage across C_P is obtained using eqn (1) and rearranging the terms.

$$|V_{cp}|_{ppu} \qquad \frac{}{2} \left| \frac{E_O}{E_{in}} \right| \quad (33)$$

The load ripple voltage is given by,

$$V_{ac} \qquad V_{crms}^2 \qquad V_c^2 \;\; ^{1/2} \quad (34)$$

V_{crms} is the total rms load voltage

V_o is the average load voltage

The Voltage ripple factor, which is a measure of the ripple content, is given by the equation

$$RF \qquad \frac{V_{ac}}{V_c} \quad (35)$$

Similarly the Voltage ripple factor using the filter elements is given by the equation

$$RippleFactor \qquad \frac{V_{2rms}}{V_c} \quad (36)$$

where V_{2rms} represents the rms value of the second harmonic component.

$$V_{2rms} \qquad \frac{V_m}{3\sqrt{2} \quad {}^2 LC} \quad (37)$$

where V_m represents the maximum value of voltage after rectification.

The efficiency of the converter is calculated using the expression

$$\% \qquad \frac{P_{out}}{P_{in}} \quad 100 \quad (38)$$

4. Performance Characteristics

In designing the full bridge series-parallel resonant converter, the given data would be the input and output voltage, output current and possibly the desired switching frequency. All other parameters of the converter need to be determined. The variables which are most important from the design point of view are normalized converter gain (E_0/Ein), normalized switching frequencies (y), peak inductor current (i_{LS}), peak series capacitor voltage (V_{cs}), peak parallel capacitor voltage (V_{cp}) etc, because they provide information to determine the component ratings. Since the graphs give more useful information than equations in understanding and designing a system, the analysis is used to obtain the design curves.

4.1 Variation of Converter Gain (E_o/E_{in}) Verses Normalized Switching Frequency (Y)

A set of characteristics has been plotted showing the variation of normalized switching frequency against voltage gain (E_0/E_{in}) with Q as a parameter using eqn.15. Figure 9 shows such characteristic curves in which the curves have been plotted for various values of Q from 1 to 6 for m=Cs/cp=1.

The curves show that normalized converter gain for a given Q increases, reaches a maximum and then decreases as the normalized switching frequency increases from 0.3 to 1.5. At higher values of Q, the normalized gain is maximum near the series resonant frequency $_o = 1 / L_sC_s$, Cs= $_o/(m+1)^{1/2}$ i.e. at normalized switching y = 0. 707. This leads to information that the load resistance is sufficiently small for high values of Q to shunt the parallel capacitor and nullify its effect on the performance

At lower values of Q, the peak of curves occurs at the frequency more than series resonant frequency. At light load, Q decreases and the effect of Cp comes in to play and as a result resonant peak moves towards higher frequency. This is because the equivalent capacitance is given by parallel combination of C_s & C_p. At sufficient light load or no load the resonant peak occurs at f_0= ½ (LCsCp/ (Cs+Cp)) $^{1/2}$ i.e. at normalized switching frequency y = 1.0.

4.2 Variation of Peak Parallel Capacitor Voltage Vs Normalized Switching Frequency.

The variation of peak parallel capacitor voltage with change in normalized switching frequency using eqn (13) is shown in Figure10. It is seen that peak parallel capacitor voltage increases with decrease in value of Q for a given frequency y and this increase is large in case of y is greater than 0.8. The frequency of operation increases up to y=1, then at that frequency, peak capacitor voltage decreases at full load but at light load it increases and this increase is much higher. Therefore this point should be taken care while designing the converter. It is observed that the peak parallel capacitor voltage for all values of Q is same at about .707pu frequency giving the peak parallel capacitor voltage of 1.4pu.

4.3 Variation of Peak Series Capacitor Voltage Vs Normalized Switching Frequency

It is observed from Figure 11. which shows the variation of peak series capacitor voltage with normalized switching frequency for different values of Q, that peak series capacitor voltage increases and attains a peak and then decreases as normalized frequency increases for a given value of Q using the eqn.26.Voltage versus normalized switching frequency for various values of Q with m = 1

These peak values get shifted to relatively higher frequency as Q decreases. An important point is that except Q = 1 maximum value of peak series capacitor voltage decreases as Q decreases and its value is same for all values of Q when per unit frequency is .88pu.

4.4 Variation of Peak Inductor Current Vs Normalized Switching Frequency

Eqn.30 shows that peak inductor current is a function of Q

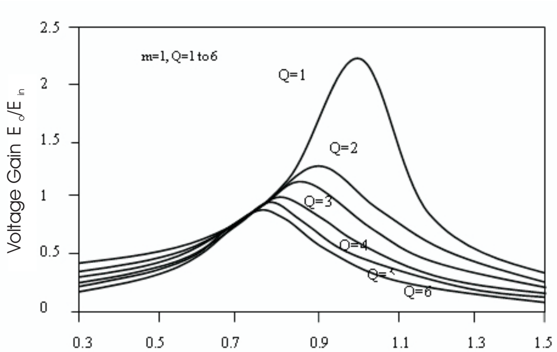


Figure 9. Variation of voltage gain versus normalized switching frequency for various values of Q with m = 1

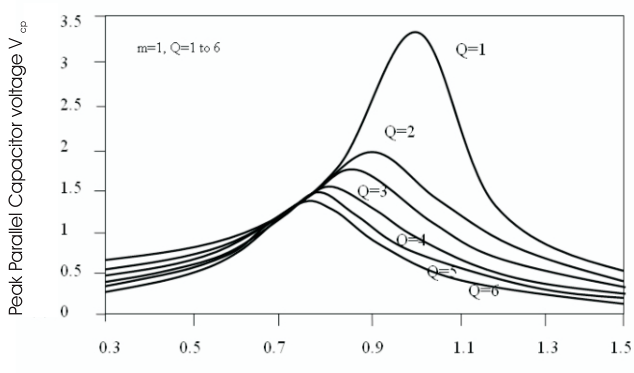


Figure10. Variation of Peak Parallel Capacitor Voltage versus normalized switching frequency for various values of with m = 1

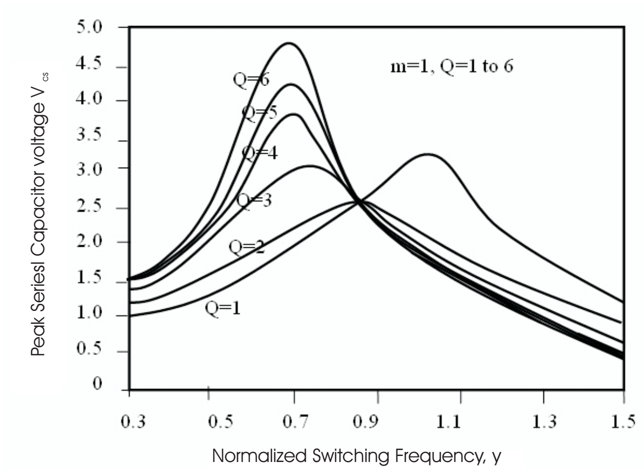


Figure 11. Variation of Peak Series Capacitor Voltage versus normalized switching frequency for various values of Q with m = 1

and y. Figure 12 shows that peak inductor current increases with increase in Q, since the output voltage decreases for the same output power. But for a given value of y, it can be seen peak current decreases as load current increases with increase in value of Q.

4.5 Variation of Duty Ratio Vs Q

In this section the qualitative analysis of the relationship between duty ratio and quality factor Q is made. Figure 13 and Figure14. show how the duty ratio D has to be varied as Q changes, to keep output load voltage constant at particular value. These curves are obtained by solving eqn.(15) numerically for duty ratio as a function of Q for various values of converter gain E_o/E_{in} (for .7 to 1.0) and

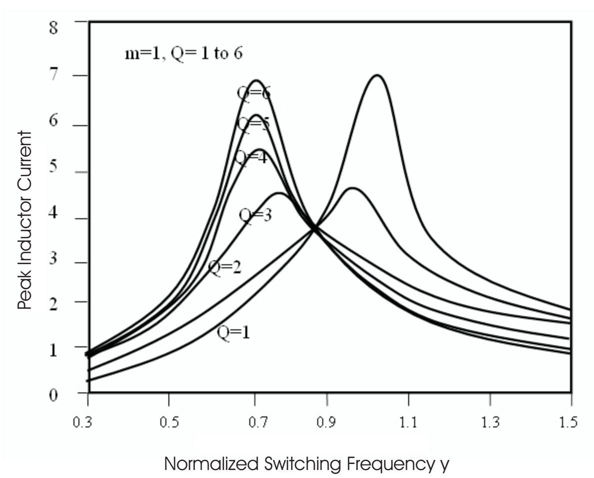


Figure12. Variation of peak inductor current versus normalized switching frequency for various values of Q with m = 1
E. Variation of Duty Ratio Vs Q

switching frequency (yield stress = 0.75 to 9). It is observed that as the E_o/E_{in} decreases, the duty ratio versus Q curves shifts downwards. The increase in value of yield stress results in shrinkage of D vs. Q curve ranges.

4.6 Variation of Converter Gain (E_o/E_{in}) Vs Normalized Switching Frequency (Y)

A set of characteristics has been plotted showing the variation of normalized switching frequency with Q as a parameter using eqn.15. Figure 14 shows one such that in which the curves have been plotted for various values of Q from 1 to 6 for m=Cs/cp=1.The curves show that normalized converter gain for a given Q increases first, reaches a maximum and then decreases as normalized switching frequency increased from .3 to 1.5.

For higher values of Q, the normalized gain is maximum

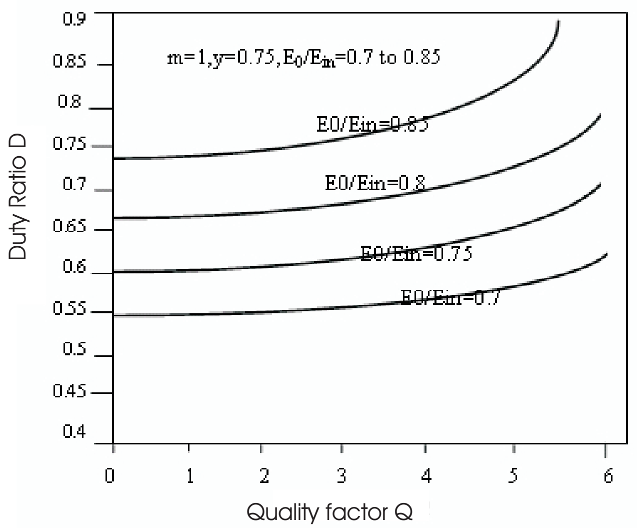


Figure 13. Variation of Duty Ratio versus Quality factor with m = 1, y = 0.75

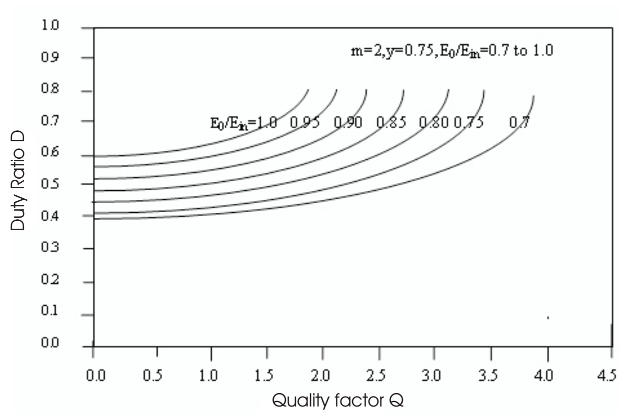


Figure 14. Variation of Duty Ratio versus Quality factor with m = 2, y= 0.75

near the series resonant frequency = 1 / (L_sC_s) ½, Cs = $_o$/(m+1)^{½} i.e. at normalized switching y = 0. 707.At lower values of Q, the peak of curves occurs at the frequency more than series resonant frequency i.e. load resistance is sufficiently small for high values of Q to shunt the parallel capacitor and nullify its effect on the performance.

At light load, Q decreases and the effect of Cp comes in to play and as a result resonant peak moves towards higher frequency. This is because the equivalent capacitance is given by parallel combination of C_s & C_p.

At sufficient light load or no load the resonant peak occurs at f= ½ (CsCp/Cs+Cp)^{½} i.e. at normalized switching frequency y = 1.0.

5. Design of Series Parallel Resonant Converter

5.1 Selection of Normalized Switching Frequency

The output voltage is regulated at all loads by proper selection of y. In Figure 13 for y = 0.75 the output voltage can be regulated at E_o/E_{in} = 0.8 for the variation in Q up to 6. But as y increases further, the range of Q up to which the converter can be regulated decreases. This implies that too high value of y cannot be chosen especially when wide load variations are expected. Besides y should not be of low value. Otherwise operation above resonance may not possible. Keeping these two factors in mind, y = 0.8 have been chosen.

5.2 Selection of Tank Circuit Q at Full Load

Size of tank depends upon the value of quality factor Q and it should not be large. Eqn(19),eqn (20),eqn(21) ,eqn (22) and eqn(30) shows that peak inductor current is a function of Q and y. Figure 12 shows that peak inductor current increases with increase in Q, since the output voltage decreases for the same output power. But for a given value of y, it can be seen that the peak inductor current decreases as load current increases with increase in value of Q. However this decrease is not drastic for values of Q greater than 5.A compromised value of Q = 5 is chosen in this design.

5.3 Selection of Normalized Converter Gain

It is clear from the circuit topology that output current is rectified and averaged tank current reflected to the secondary side of the transformer. Since the tank current is directly related to the output current, therefore we should choose a large conversion ratio, so that the turns ratio is minimized, resulting in the smallest possible tank current on the primary for a specified output current on the secondary. Hence the conversion ratio should be chosen close to one. Based on above consideration, the following optimum values are selected in the design of the converter.

Normalized frequency y = 0.8.

Cs/Cp ratio m = 1

Q of tank circuit at full load = 5

$$\left|\frac{E_0}{E_{in}}\right| \quad 0.8$$

Design

Input voltage E_{in} = 30 volts

Output voltage E_o =24 volts

Output Current = 1.5 Amps

Switching frequency = 50 kHz

m=C_s/C_p = 1, Q=5, y=0.8

Load resistance R=V_0/I_0=16

$$R \quad \frac{_0 L}{Q} \quad \frac{1}{Q} \quad \sqrt{\frac{L}{C}}$$

Resonant frequency f_o is given by

f_o = f/y = 50,000/0.8 = 62.5 kHz

But $$\sqrt{\frac{L}{C}} \quad Q \quad R \quad 5 \quad 16 \quad 80$$

$$f_0 \quad \frac{1}{2 \quad \sqrt{LC}}$$

$$\frac{1}{\sqrt{LC}} \quad 2 \quad 62.5 \quad 10^{3}$$

The values of L & C are L = 204 H and C = 0.0318 F

Since Cs = Cp,Cs = Cp = 2C = 0.0636 F

If Cs = Cp =0.047 F is selected for the purpose of standard available capacitance then L=261mH.

6. Experimental Results

Some testing results are presented in this section to verify the theoretical predictions of previous sections. An experimental prototype has been implemented for a resistive load as shown in Figure 15. The load rating is 24V, 36W. The resonant inductor is 0.261mH and the inductor is wound around ferrite core and the series resonant capacitor is 0.47 F and the capacitor used is of polypropylene film type.

The switching frequency is 50KHz.All the four switches used is of IRF460 with an external fast recovery diode BYE26E connected across each switching device. In the secondary side, the diodes used for rectification are FR306.The filter inductor is 40 H and is wound around ferrite core. The filter capacitance is 100 F, 63V and the capacitor used is of electrolytic type. Figure 16 to Figure18 shows the experimental output obtained. In each Figure,(a) shows the voltage across the series capacitor and (b) shows the output voltage across the load after connecting the filter elements.

Table1&2 gives the Comparison of Results between Calculated and experimental results respectively of Series Parallel Resonant Converter for a input D-C supply Voltage of 30V and Switching Frequency of 50 kHz.

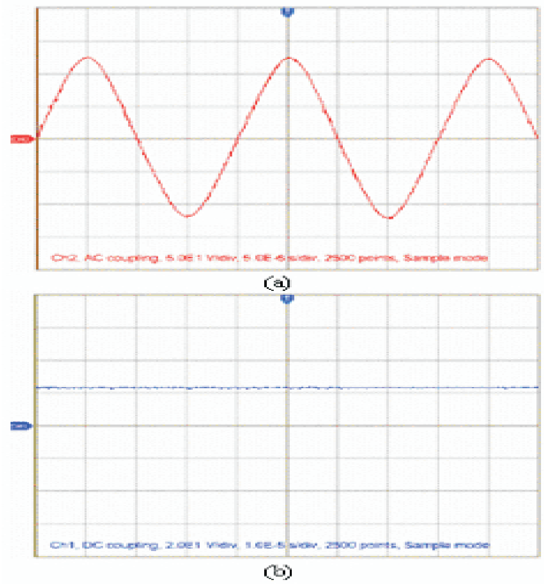


Figure 16. Experimental results for series parallel resonant converter at full load with m=1: (a) V_{cs}, (b) V_0 with filter

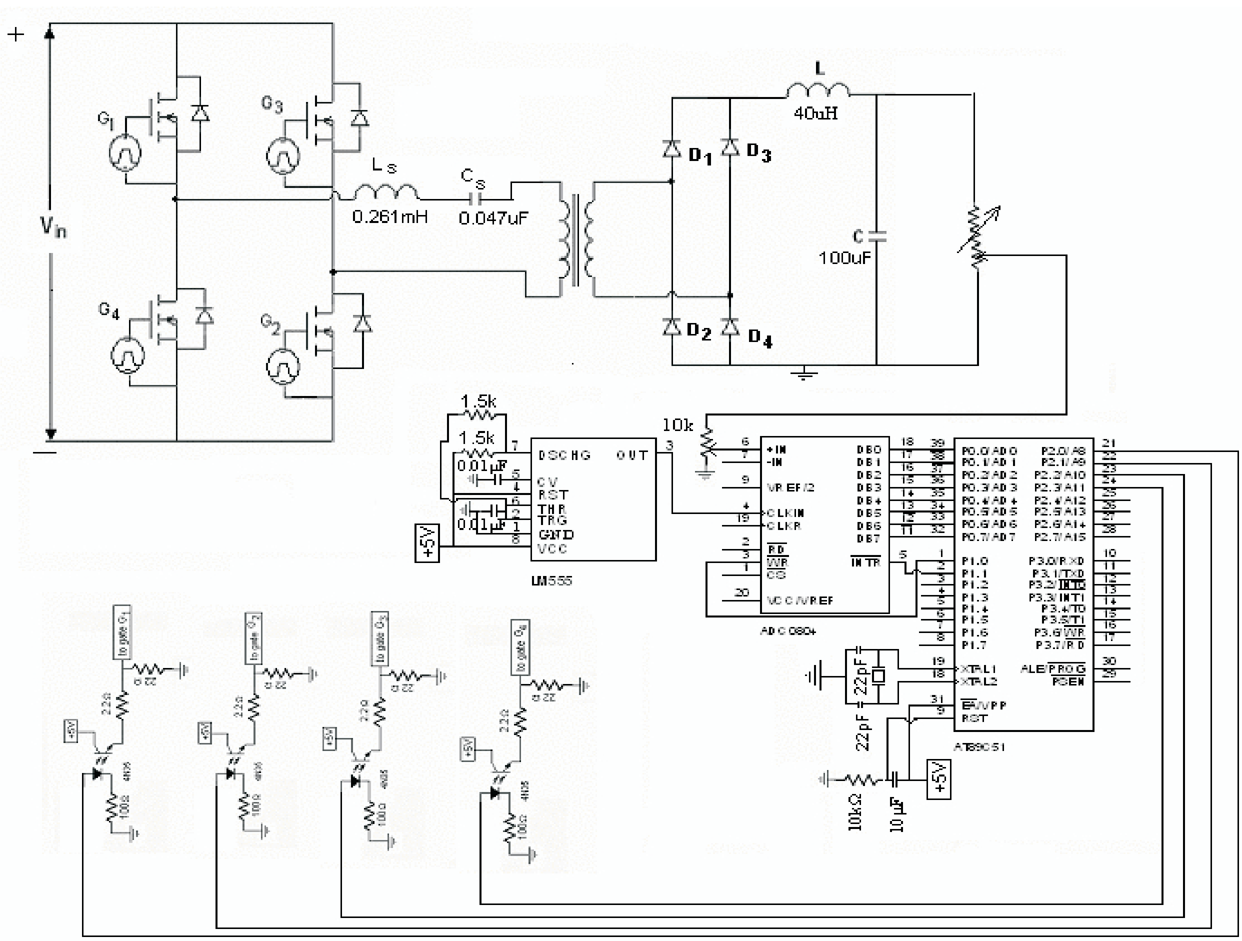


Figure 15. Experimental circuit

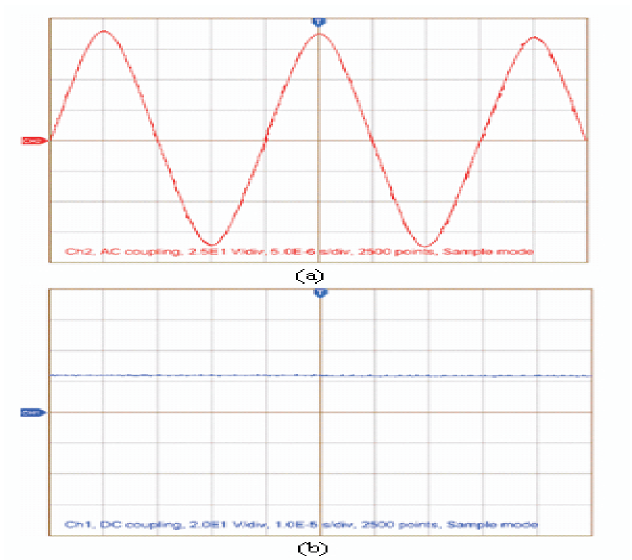


Figure17. Experimental results for series parallel resonant converter at 70% load with m=1: (a) V_{cs}, (b) V_0 with filter

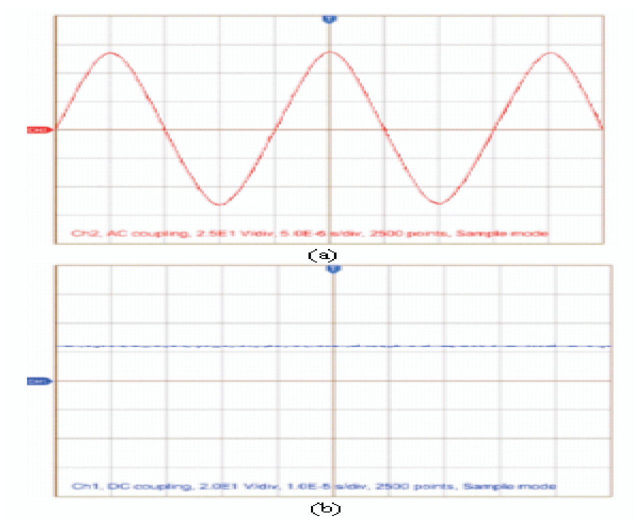


Figure 18. Experimental results for series parallel resonant converter at 40% load with m=1: (a) V_{cs}, (b) V_0 with filter

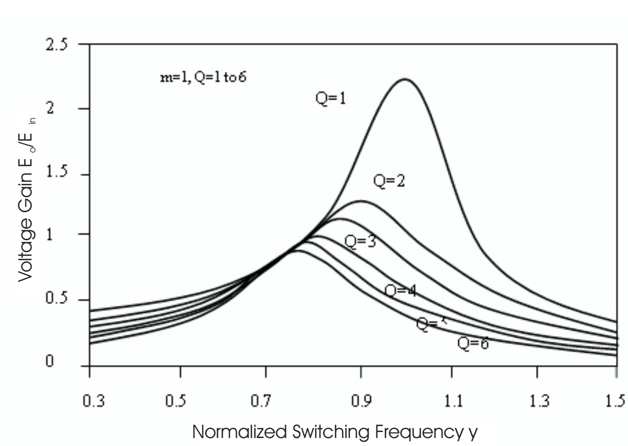


Figure 19. Variation of voltage gain versus normalized switching frequency for Various values of Q

Table 3 - Efficiency obtained for Series Parallel Resonant Converter for I/P D-C supply Voltage = 30 V and Switching Frequency = 50 kHz

Table 4 - Efficiency obtained with conventional method

Load %	Duty Ratio D	Series capacitor voltage Vcp(peak) volts	Series inductor voltage Vcs(peak) volts	Output current I_o amps	Output voltage Y_o volts	Ripple Factor without filter %	Ripple Factor withfilter %
100	0.9	116.6	149.7	1.5	24	20.2	0.0055
90	0.86	104.85	134.2	1.35	24	19.8	0.0047
80	0.79	93.2	117.5	1.2	24	18.9	0.0036
70	0.72	81.55	104.4	105	24	17.5	0.0024
60	0.63	69.9	89.5	0.09	24	16.9	0.0017
40	0.45	58.25	59.6	0.06	24	15.3	0.0008

Table1. Calculated Results

Load %	Duty Ratio D	Series capacitor voltage Vcp (peak) volts	Series inductor voltage Vcs (peak) volts	Output currentI_o amps	Output voltage V_o volts	Ripple Factor without filter %	Ripple Factor with filter %
100	0.92	126.6	166.1	1.5	24	21.8	0.0065
90	0.88	115.6	145.5	1.35	24	20.9	0.0056
80	0.8	102.3	132.1	1.2	24	19.6	0.0048
70	0.73	92.9	118.1	1.05	24	18.5	0.0035
60	0.63	76.5	105.2	0.9	24	17.2	0.0025
40	0.44	64.4	84.6	0.6	24	16.4	0.0012

Table2. Experimental results

Duty Ratio	Input current (amps)	Input voltage (volts)	Output current (amps)	Output voltage (volts)	Efficiency %
1	1.81	30	1.5	33.27	91.9
1	1.65	30	1.35	33.65	91.77
1	1.49	30	1.2	33.81	90.74
1	1.33	30	1.05	34.02	89.47
1	1.17	30	0.9	34.71	89
1	1.02	30	0.75	35.64	87.42

Table3. Experimental Results

Duty Ratio	Input Current (amps)	Input Voltage (volts)	Output current (amps)	Output current (volts)	Efficiency 96
1	1.63	30	1.5	26.94	82.65
1	1.49	30	1.35	27.28	82.29
1	1.35	30	1.2	27.53	81.76
1	1.19	30	1.05	27.86	81.53
1	1.04	30	0.9	28.17	81.14
1	0.88	30	0.79	28.34	80.67

Table 4. Experimental Results

for variable I/P D-C supply Voltage and Switching Frequency = 50 kHz

Conclusion

A new high frequency regulation method for a DC-DC converter is presented that permits the implementation of a voltage control strategy Regulation is achieved by varying the conduction angle of the switching devices. The switches are operated under zero current conditions and therefore result in much higher efficiency and reduced voltage stresses. The regulation principle is general and can be implemented in any kind of converter without modifying its operation. Based on the converter analysis, characteristic curves have been obtained and a step-by-step design procedure of the converter has been given. The proposed method is having better efficiency than the conventional method. Results obtained from the prototype verify the feasibility and the advantages of the topology.

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