A NOVEL AND UNIVERSAL PULSE WIDTH MODULATION TECHNIQUE FOR CASCADED MULTILEVEL INVERTERS

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ABSTRACT

A Space Vector Pulse Width Modulation (SVPWM) scheme for cascaded multilevel inverters is proposed in this paper. The proposed PWM scheme generates the inverter leg switching times, from the sampled reference phase voltage amplitudes and centres the switching times for the middle vectors, in a sampling interval, as in the case of conventional space vector PWM (SVPWM). The SVPWM scheme, presented for diode clamped multilevel inverters, can also work in the overmodulation range, using only the sampled amplitudes of reference phase voltages. The present PWM technique does not involve any sector identification and considerably reduces the computation time when compared to the conventional space vector PWM technique. The present PWM signal generation scheme can be used for any multilevel inverter configuration.

Keywords: Cascaded Multilevel Inverter, THD, Sine Pulse Width Modulation, Space Vector Pulse Width Modulation.

INTRODUCTION

The two most widely used PWM schemes for cascaded multilevel inverters are the carrier-based sine-triangle PWM (SPWM) technique and the space vector PWM (SVPWM) technique. These modulation techniques have been extensively studied and compared for the performance parameters with two-level inverters [1]-[2]. The SPWM schemes are more flexible and simpler to implement, but the maximum peak of the fundamental component in the output voltage is limited to 50% of the DC link voltage [2], and the extension of the SPWM schemes into the over-modulation range is difficult. In SVPWM schemes, a reference space vector is sampled at regular intervals to determine the inverter switching vectors and their time durations, in a sampling interval. The SVPWM scheme gives a more fundamental voltage and better harmonic performance compared to the SPWM schemes [3]–[5]. The maximum peak of the fundamental component in the output voltage obtained with space vector modulation is 15% greater than with the sine-triangle modulation scheme [2]-[3]. But the conventional SVPWM requires sector identification and look-up tables to determine the timings for various switching vectors of the inverter, in all the sectors [3]-[4]. This makes the implementation of the SVPWM scheme quite complicated. A SVPWM scheme, extending the modulation range into the overmodulation range, has been presented [6]-[7], in which extensive offline computations and look-up tables are required, to determine the modified reference vector, in the overmodulation range, extending up to six-step operation. It has been shown that, for two-level inverters, a SVPWM- like performance can be obtained with a SPWM scheme by adding a common mode voltage of suitable magnitude, to the sinusoidal reference phase voltage. A simplified method, to determine the correct offset times for centering the time durations of the middle inverter vectors, in a sampling interval, is presented [8], for the two-level inverter. The inverter leg switching times are calculated directly from the sampled amplitudes of the reference three-phase voltages with considerable reduction in the computation time [8].

The SPWM technique, when applied to multilevel inverters, uses a number of level-shifted carrier waves to compare with the reference phase voltage signals [9]. The SVPWM for multilevel inverters [10]-[11] involves mapping of the

outer sectors to an inner sub hexagon sector, to determine the switching time duration, for various inverter vectors. Then the switching inverter vectors corresponding to the actual sector are switched, for the time durations calculated from the mapped inner sectors. It is obvious that such a scheme, in multilevel inverters, will be very complex, as a large number of sectors and inverter vectors are involved. This will also considerably increase the computation time.

A modulation scheme is presented in [12]-[13], where a fixed common mode voltage, is added to the reference phase voltage throughout the duration range. It has been shown that this common mode addition will not result in a SVPWM-like performance, as it will not centre the middle inverter vectors in a sampling interval. The common mode voltage to be added in the reference phase voltages, to achieve SVPWM-like performance, is a function of the modulation index for multilevel inverters. A SVPWM scheme based on the above principle has been presented [14], where the switching time for the inverter legs is directly determined from sampled phase voltage amplitudes. This technique reduces the computation time considerably more than the conventional SVPWM techniques do, but it involves region identifications based on modulation indices. While this SVPWM scheme works well for a three-level PWM generation, it cannot be extended to multilevel inverters of levels higher than three, as the region identification becomes more complicated. A carrier-based PWM scheme has been presented [15], where sinusoidal references are added with a proper offset voltage before being compared with carriers, to achieve the performance of a SVPWM. The offset voltage computation is based on a modulus function depending on the DC link voltage, number of levels and the phase voltage amplitudes. The implementation details and the operation of the proposed method in the overmodulation region remain unaddressed.

The objective of this paper is to present an implementation scheme for PWM signal generation for multilevel inverters, similar to the SVPWM scheme, for the entire range of modulation indices including overmodulation. The PWM switching times for the inverter legs are directly derived from the sampled amplitudes of the reference phase voltages. The SVPWM switching pattern generation is not realised with offset voltage computation from a modulus function [15]. A simple way of adding a time offset to the inverter-gating signal, to generate the SVPWM pattern, from only the sampled amplitudes of reference phase voltages, is explained. The proposed SVPWM signal generation does not involve checks for region identification, as in the SVPWM scheme presented in [14]. Also, the algorithm does not require either sector identification or look-up tables for switching vector determination as are required in the conventional multilevel SVPWM schemes [10]-[11]. Thus the scheme is computationally efficient when compared to conventional multilevel SVPWM schemes, making it superior for real-time implementation. The proposed SVPWM algorithm can easily be extended to any multilevel inverter configurations. For experimental verification of the proposed SVPWM scheme, we are using a five-level inverter.

1. Proposed SVPWM

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other [1].

To obtain the maximum possible peak amplitude of the fundamental phase voltage, in linear modulation, a common mode voltage, $V_{offset1}$, is added to the reference phase voltages [5],[12] where the magnitude of $V_{offset1}$ is given by,(Figure 1).

$$V_{offset1} = -(V_{max} + V_{min})/2 \qquad (1)$$

Where,

V_{max} = Maximum magnitude of the three sampled reference phase voltages, in a sampling interval.

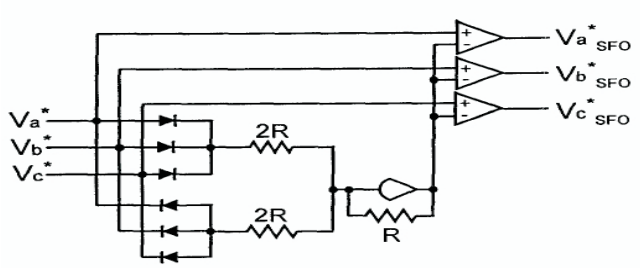

Figure1. Calculation of $V_{offset1}$ from phase voltage samples

V_{min} = Minimum magnitude of the three sampled reference phase voltages, in a sampling interval.

i.e. $V_{max} = \max(V_{an}, V_{bn}, V_{cn})$

$V_{min} = \min(V_{an}, V_{bn}, V_{cn})$

The addition of the common mode voltage, $V_{offset1}$, results in the active inverter switching vectors being centered in a sampling interval, making the SPWM technique equivalent to the SVPWM technique [3]. Equation (1) is based on the fact that, in a sampling interval, the reference phase which has lowest magnitude (termed the min-phase) crosses the triangular carrier first and causes the first transition in the inverter switching state. While the reference phase, which has the maximum magnitude (termed the max-phase), crosses the carrier last and causes the last switching transition in the inverter switching states in a two-level SVPWM scheme [5], [13].

Thus the switching periods of the active vectors can be determined from the (max-phase and min-phase) sampled reference phase voltage amplitudes in a two-level inverter scheme [8]. The SPWM technique, for multilevel inverters, involves comparing the reference phase voltage signals with a number of symmetrical level-shifted carrier waves for PWM generation. It has been shown that for an n-level inverter, n-1 level-shifted carrier waves are required for comparison with the sinusoidal references [9]. Because of the level-shifted multicarriers as shown in Figure 2, the first crossing (termed the first-cross) of the reference phase voltage cannot always be the min-phase. Similarly, the last crossing (termed the third-cross) of the reference phase voltage cannot always be the max-phase. Thus the offset voltage computation, based on eqn. (1) is not sufficient to centre the middle inverter switching vectors, in a multilevel PWM scheme during a sampling period T_s shown in Figure 3. In this, a simple technique to determine the offset voltage (to be added to the reference phase voltage for PWM generation for the entire modulation range) is presented, based only on the sampled amplitudes of the reference phase voltages.

The proposed scheme is to determine the sampled reference phase, from the three sampled reference

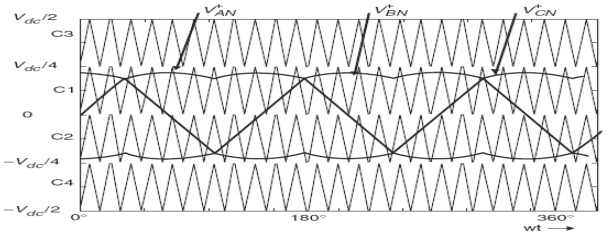

Figure 2. Reference voltages and triangular carriers for a Five-level PWM scheme

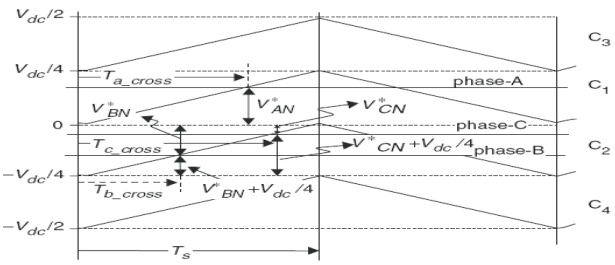

Figure 3. Determination of the $T_{a\ cross}$, $T_{b\ cross}$ and $T_{c\ cross}$ during switching interval T_s (Mi=0.433)

phases, which crosses the triangular first (first-cross) and the reference phase which crosses the triangular carrier last (third-cross). Once the first-cross phase and third-cross phase are identified, the principles of offset calculation by eqn. (1), for the two-level inverter, can easily be adapted for the multilevel SVPWM generation scheme. The proposed SVPWM technique presents a simple way to determine the time instants at which the three reference phases cross the triangular carriers.

These time instants are sorted to find the offset voltage to be added to the reference phase voltages for SVPWM generation for multilevel inverters for the entire linear modulation range, so that the middle inverter switching vectors are centered (during a sampling interval), as in the case of the conventional two-level SPWM scheme.

2. Determination of Inverter Leg Switching Times

The Figure 2 shows a reference voltage and four triangular carriers used for PWM generation for a five-level inverter. The modified reference phase voltages are given by

$$V^*_{XN} = V^{XN} + V_{offset1}, X = A, B, C \quad (2)$$

Where,

V_{AN}, V_{BN}, V_{CN} = Sampled amplitudes of three reference phase voltages during the current sampling interval.

The reference phase voltages are equally spaced between the four carriers as shown in Figure 2, for a five-

level inverter. For modulation indices less than 0.433 (half of the maximum Modulation Index(MI) in the linear range of modulation for a five-level inverter), the reference phase voltage spans inner two carriers. For modulation indices higher than 0.433, the reference phase voltages expand into the outer carrier regions. The addition of $V_{offset1}$, obtained from eqn. (1), to the reference phase voltage ensures that the modified reference voltages always remain within the carrier regions through the linear modulation range (maximum MI in the linear modulation range is 0.866) [3].

The reference phase voltages cross the triangular carriers at different instants in a sampling period T_s shown in Figure 3. Each time a reference phase voltage crosses the triangular carrier and it causes a change in the inverter state. The phase voltage variations and their time durations are shown in Figure 3. The sampling time interval T_s, can be divided into four time intervals T_{01}, T_1, T_2 and T_{03}. T_{01} and T_{03} are defined as the time durations for the start and end inverter switching vectors respectively, in a sampling time interval T_s. T_1 and T_2 are defined as the time durations for the middle inverter switching vectors, in a sampling time interval T_s. It should be noted from Figure 3 that the middle switching vectors are not centred in a sampling interval T_s. So an additional offset (offset2) needs to be added to the reference phase voltages of Figure 1, so that the middle inverter switching vectors can be centred in a sampling interval, similar to a two-level SVPWM [3].

The time duration, at which the A-phase crosses the triangular carrier, is defined as $T_{a\ cross}$. Similarly, the time durations, when the B-phase and C-phase cross the triangular carrier, are defined as $T_{b\ cross}$ and $T_{c\ cross}$, respectively. Figure 3 shows a sampling interval when the A-phase is in the carrier region C1 while the B-phase and C- phase are in carrier region C2, the time duration, $T_{a\ cross}$, (measured from the start of the sampling interval) at which the A-phase crosses the triangular carrier is directly proportional to the phase voltage amplitudes, V_{AN} . The time duration, $T_{b\ cross}$, at which the B-phase crosses the triangular carrier, is proportional to V^*_{BN} $\frac{V_{DC}}{4}$ and the time duration, T_c cross, at which the C-phase crosses the triangular carrier, is proportional to V^*_{CN} $\frac{V_{DC}}{4}$ Therefore

$$T_{c\_cross} \quad V^*_{CN} \quad \frac{V_{DC}}{4} * \frac{T_s}{\frac{V_{DC}}{4}} \quad T^*_{cs} \quad T_s \qquad (3)$$

$$T_{b\_cross} \quad V^*_{BN} \quad \frac{V_{DC}}{4} * \frac{T_s}{\frac{V_{DC}}{4}} \quad T^*_{bs} \quad T_s \qquad (4)$$

$$T_{a\_cross} \quad V^*_{AN} \quad \frac{V_{DC}}{4} \quad T^*_{as} \qquad (5)$$

Where,

T^*_{as} T^*_{bs} T^*_{cs} = Time equivalents of the phase voltage magnitudes.

The Proportionality between the time equivalents and corresponding voltage magnitudes is defined as follows [8]:

$$\frac{\frac{V_{DC}}{4}}{T_s} \quad \frac{V^*_{AN}}{T^*_{as}}$$

$$\frac{\frac{V_{DC}}{4}}{T_s} \quad \frac{V^*_{BN}}{T^*_{bs}}$$

$$\frac{\frac{V_{DC}}{4}}{T_s} \quad \frac{V^*_{CN}}{T^*_{cs}}$$

The Figure 4 shows the situation, where the reference phase voltages span the entire carrier region, for a five-level inverter scheme. The time durations, at which the reference phase voltages cross the carrier, can be similarly determined.

As shown in Figure 3, T_{across} is proportional to V^*_{AN} $\frac{V_{DC}}{4}$ whereas T_{bcross} is proportional to V^*_{BN} $\frac{V_{DC}}{2}$ and T_{ccross} is proportional to V^*_{CN} $\frac{V_{DC}}{4}$ Therefore, from eqn. (4)

$$T_{first\ cross} = \min (T_{x\ cross}),$$

$$T_{second\ cross} = \text{mid}\ (T_{x\ cross}),$$

$$T_{third\ cross} = \max (T_{x\ cross}), \quad X = a, b, c \qquad (6)$$

In the present work, the $T_{a\ cross}$, $T_{b\ cross}$ and $T_{c\ cross}$ time durations obtained above are used to centre the middle switching vectors, as in the case of two-level inverters, in a sampling interval T_s [8]. The time duration, at which the reference phases cross the triangular carriers for the first time, is

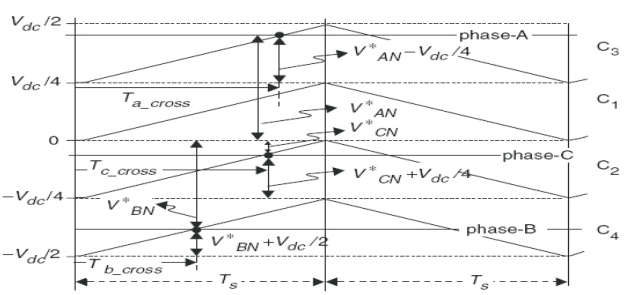

Figure 4. Determination of the $T_{a\ cross}$, $T_{b\ cross}$ and $T_{c\ cross}$ during switching interval T_s(Reference voltages span the entire carrier region, 0.433<Mi< 0.866)

defined as $T_{first\ cross}$. Similarly, the time durations, at which the reference phases cross the triangular carriers for the second and third time, are defined as, $T_{second\ cross}$ and $T_{third\ cross}$, respectively, in a sampling interval T_s. The time durations, $T_{first\ cross}$, $T_{second\ cross}$ and $T_{third\ cross}$, directly decide the switching times for the different inverter voltage vectors, forming a triangular sector, during one sampling interval T_s. The time durations for the start and end vectors, are $T_{01} = T_{first\ cross}$, $T_{03} = T_s - T_{third\ cross}$, respectively as shown in Figure 3. The middle vectors are centred by adding a time offset, $T_{offset2}$ to $T_{first\ cross}$, $T_{second\ cross}$ and $T_{third\ cross}$. The time offset, $T_{offset2}$ is determined as follows. The time duration for the middle inverter switching vectors, T_{middle}, is given by,

$$T_{middle} = T_{third\ cross} - T_{first\ cross} \quad (7a)$$

The time duration of the start and end vector is,

$$T_0 = T_s - T_{middle} \quad (7b)$$

Thus the time duration of the start vector is given by,

$$T_0/2 = T_{first\ cross} + T_{offset2}$$

Therefore,

$$T_{offset2} = T_0/2 - T_{first\ cross} \quad (7c)$$

The addition of the time, $T_{offset2}$ to $T_{a\ cross}$, $T_{b\ cross}$ and $T_{c\ cross}$ gives the inverter leg switching times T_{ga}, T_{gb} and T_{gc} for phases A, B and C, respectively.

$$\begin{aligned} T_{ga} &= T_{a\,cross} + T_{offset2} \\ T_{gb} &= T_{b\,cross} + T_{offset2} \\ T_{gc} &= T_{c\,cross} + T_{offset2} \end{aligned} \quad (8)$$

The traces of different timing signals, for the proposed PWM scheme, are shown in Figure 5. to Figure 7., for a five-level PWM generation. The traces of $T_{a\ cross}$ for various modulation indices are shown in Figure 5. The traces of $T_{first\ cross}$, $T_{second\ cross}$ and $T_{third\ cross}$ are shown in Figure 6a. while the traces of $T_{gfirst\ cross}$, $T_{g\ second\ cross}$ and $T_{g\ third\ cross}$ are shown in Figure 6b. It can be seen from Figure 6b, that the time durations

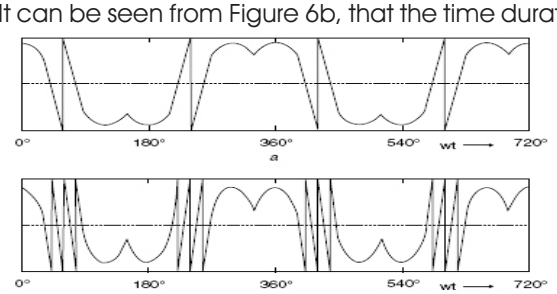

Figure 5. Trace of $T_{a\ cross}$ for modulation indexes 0.41 and 0.8

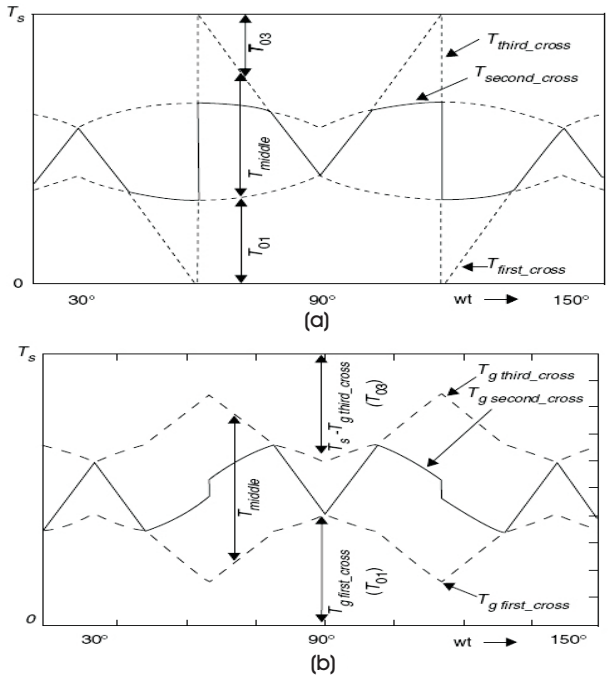

Figure 6. Traces of $T_{first\ cross}$, $T_{second\ cross}$ and $T_{third\ cross}$ a non-centred time duration for middle vectors b centred time duration for middle vectors, after addition of required offset, T_offset2

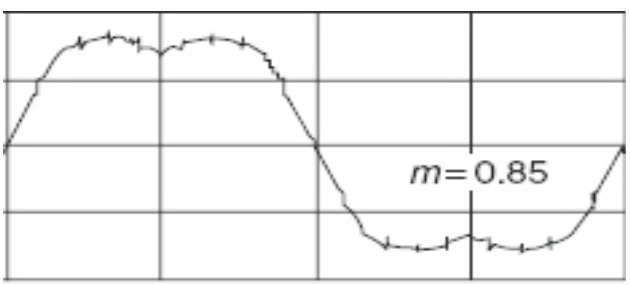

Figure 7. Modulation indices profile of Toffset1 + Toffset2 for modulation index=0.85

3. Simulation Results (Figures 8-13)

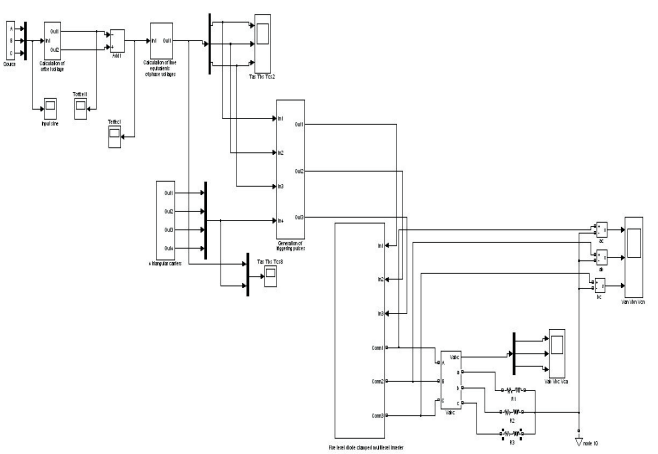

Figure 8. Matlab/Simulink Model of a Three Phase Five Level Cascaded Multilevel Inverter

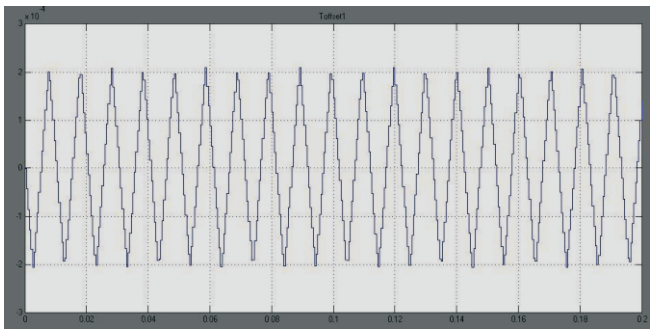

Figure 9. Offset Voltage Waveform

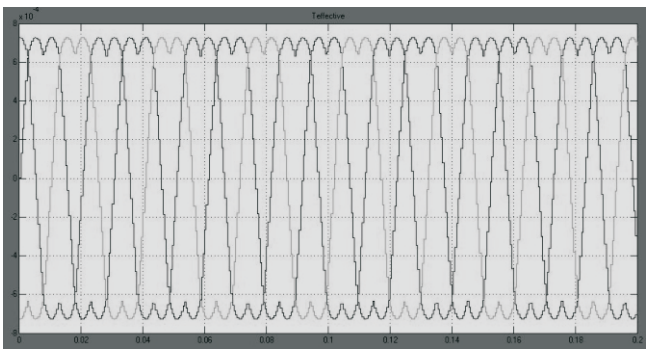

Figure 10. Effective Voltage Waveform

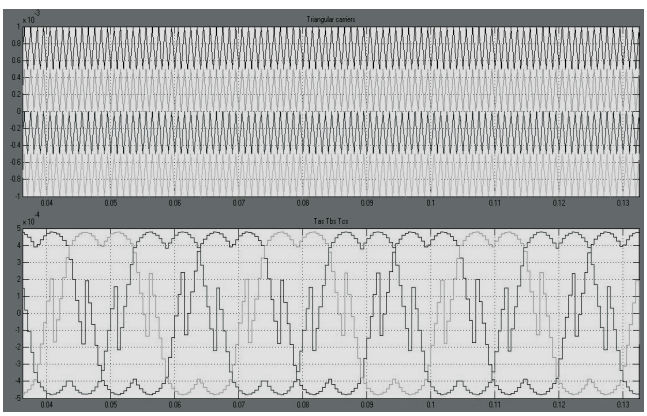

Figure 11. The Four Triangular Waveforms and the Time Equivalents of The Phase Voltages

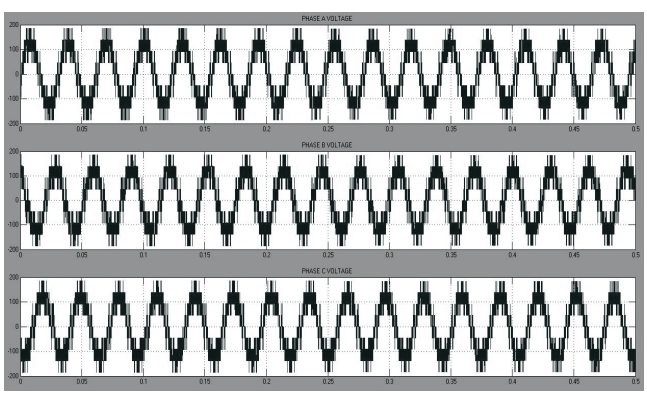

Figure 12. Phase Voltage Waveforms

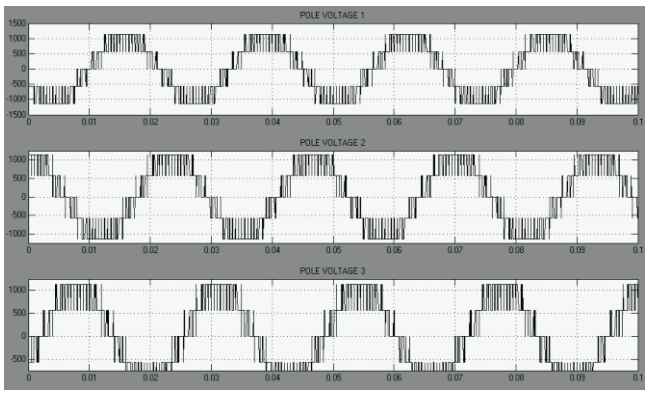

Figure 13. Line Voltage Waveforms

for the start vector ($T_{g\ first\ cross}$) and for the end vector (T_s - $T_{g\ third\ cross}$) are equal. Thus the middle vectors are always centred, in a sampling time interval T_s. The plots of the time equivalent of the modified reference phase voltage, $T_{offset1} + T_{offset2}$, for modulation index 0.85 is shown in Figure 7. The corresponding traces of the total offset, $T^*_{as} + T_{offset2}$, added to the sinusoidal reference phase voltage to make the SPWM equivalent to the SVPWM, are shown in Figure 7.

Conclusions

A voltage modulation scheme of the SVPWM has been presented for cascaded multilevel inverter. The centring of the middle inverter switching vectors of the SVPWM is achieved by the addition of an offset time signal to the inverter gating signals, derived from the sampled amplitudes of the reference phase voltages. The proposed SVPWM scheme covers the entire modulation range, including the overmodulation region. The PWM technique, presented in this paper, does not need, any sector identification, as the case in conventional SVPWM schemes. Complicated calculations for inverter switching vector times and look-up tables for selecting the inverter switching vectors are also avoided in this proposed method. This reduces the computation time, required to determine the switching times for inverter legs, memory requirement of the digital processors making the algorithm suitable for real-time implementation. The proposed SVPWM signal generation can be applied to any multilevel inverter configurations. In the present work, a five-level cascaded multilevel inverter is used for experimental verification of the proposed technique, and the experimental results validation is in progress with the

proposed algorithm.

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Appendix

Algorithm for Inverter Leg Switching Time Calculation for a n-level Inverter Scheme

(1) Read the sampled amplitudes of V_{AN}, V_{BN} and V_{CN} for the current sampling interval

(2) Determine the time equivalents of phase voltages, i.e. T_{as}, T_{bs} and T_{cs}.

(3) Find $T_{offset1}$ using T_{max} and T_{min}, T_{max}, T_{min} are the maximum and minimum of T_{as}, T_{bs} and T_{cs}.

(4) Determine $T_{effective}$.

(5) Determine $T_{a\,cross}$, $T_{b\,cross}$ and $T_{c\,cross}$.

(6) Sort $T_{a\,cross}$,$T_{b\,cross}$ and $T_{c\,cross}$ to determine $T_{first\,cross}$,$T_{second\,cross}$ and $T_{third\,cross}$,The maximum of $T_{a\,cross}$,$T_{b\,cross}$ and $T_{c\,cross}$ is $T_{third\,cross}$. The minimum of $T_{a\,cross}$,$T_{b\,cross}$ and $T_{c\,cross}$ is $T_{first\,cross}$,and theremaining one is $T_{second\,cross}$.

(7) Assign first_cross_phase, second_cross_phase and third_cross_phase according to the phase which determines$T_{first\,cross}$,$T_{second\,cross}$ and $T_{third\,cross}$.

(8) Determine T_{ga}, T_{gb} and T_{gc}.

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