EFFICIENT REALIZATION OF REVERSIBLE GRAY TO BINARY CODE CONVERTER CIRCUIT

By

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ABSTRACT

In present years, reversible logic has attained importance in many applications in the field of Quantum Computing, Nanotechnology, Low Power CMOS Design, Cryptography, etc. Without reversible logic, it is not possible to realize quantum computing. Code converters are combinational circuits which are used in digital systems designed to enhance the security of data and to decrease the hardware complexity. This paper presents a design for the reversible gray to binary code converter circuit. The main aim in the reversible logic design is to minimize the number of reversible gates used and the garbage output produced. The proposed design is compared to the existing designs in terms of parameters such as reversible gates, constant inputs, garbage outputs, and quantum cost.

Keywords: Reversible Logic, Reversible Gray Code to Binary Code Converters.

INTRODUCTION

In digital circuits, the data are denoted as a group of bits ('0' and '1') known as code. A code is the combination of 0's and 1's to represent the information. A logic circuit which is useful to convert information in one form to another form is known as code converter. In digital domain, different codes are available such as ASCII, Binary Sequence, Gray, Octal, etc. Conversion of code from one format to another format is a prominent process while performing the operations in digital systems such as microprocessor, digital signal processor, etc.

Earlier in 1961, R. Landauer has shown that every bit of information loss will dissipate energy in the form of heat [1]. Later in 1973, C.H. Bennett has proved that the energy loss in a circuit can be ideally decreased to zero, by using reversible logic gates for the designing of circuits [2].

1. Design Constraints of Reversible Logic

A reversible gate is a m-inputs and m-outputs logic circuit in which there is a one to one mapping between input vectors and output vectors. Some important reversible gates are shown in Table 1. Few main parameters which play a major role in reversible circuit design are listed below.

- *Gate Count*: Number of reversible logic gates needed to realize the given function.
- *Constant Inputs:* Inputs of a reversible gate to be maintained at a constant value of '0' or '1' in order to obtain the given required boolean function is known as constant inputs.
- *Garbage Outputs:* The extra outputs in the reversible logic circuits that maintains the reversibility and do not carry out any useful operation is called as garbage outputs.
- *Quantum Cost:* Reversible logic gates can be implemented using 1x1 and 2x2 reversible gates. These gates are known as primitive gates. The quantum cost of the reversible circuit can be calculated in terms of cost of primitive reversible gates.

2. Reversible Gray to Binary Code Converter Circuits Designs

Till today only few researchers have worked in the area of designing a gray to binary code converter using reversible logic approach. In 2013, M. Saravanan and M. Suresh Manic presented the reversible gray to binary code converter using five Feynman gates [3] shown in Figure 1 [6]. This design requires two constant inputs and produce three garbage outputs. Quantum cost of this design was evaluated as five. Later in 2014, Kotaiah Kamani et al.

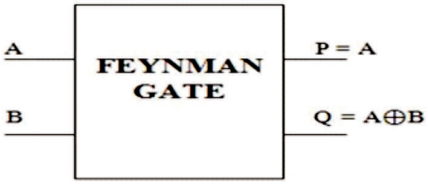
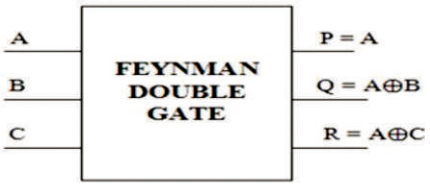
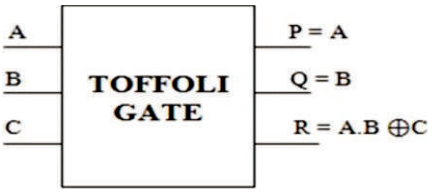
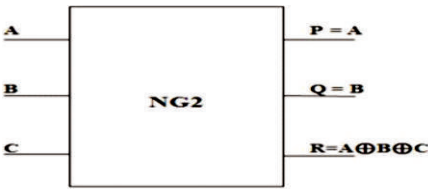
Reversible Gate	Diagrammatic Representation	Size	Inputs	Outputs
Feynman Gate (FG) [3]		2x2	A, B	P, Q P = A, Q = A⊕B
Feynman Double Gate (F2G) [4]		3x3	A, B, C	P, Q, R P = A, Q = A⊕B, R = A⊕C
Toffoli Gate (TG) [5]		3x3	A, B, C	P, Q, R P = A, Q = B, R = A.B⊕C
NG1 [7]		3x3	A, B, C	P, Q, R P = A, Q = A⊕B, R = A⊕B⊕C
NG2 [7]		3x3	A, B, C	P, Q, R P = A, Q = B, R = A⊕B⊕C

Table 1. Existing Reversible Gates

proposed new reversible logic gates named as NG1 and NG2 of 3x3 size. They have designed a gray to binary code converter with reversible approach using a combination of NG1 and NG2. This circuit has used two reversible logic gates as shown in Figure 2 and the quantum cost of this circuit has not reported in the literature [7].

This paper proposes a design for gray to binary code converter circuit using reversible logic gates as shown in Figure 3. The proposed design uses two reversible gates. The reversible gates used in the design are NG1 and Feynman. This design does not need any constant inputs and generates no garbage outputs.

3. Results and Analysis of the Design

The proposed reversible gray to binary code converter circuit was logically verified through simulations as shown in Figure 4. The Verilog HDL is used to code the proposed reversible design, the test benches are created and simulations are made to verify the correctness of the proposed design.

Conclusion

This paper shows the gray to binary code converter circuit implemented using NG1 and Feynman reversible logic gates. The logical correctness of the proposed design were verified using Verilog Hardware description language in Xilinx 14.1. The parameters of the proposed design were evaluated and compared with the existing designs in terms of number of reversible gates used, constant inputs applied, garbage outputs generated and quantum cost of

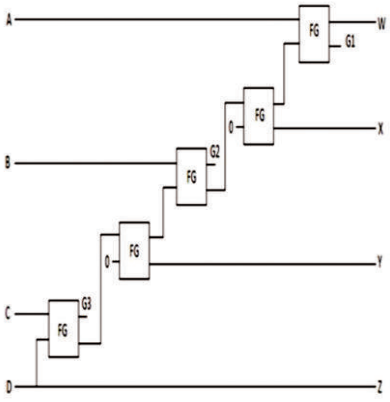


Figure 1. Existing Design 1

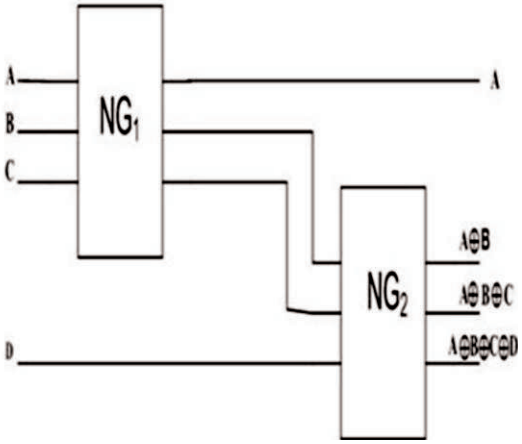


Figure 2. Existing Design 2

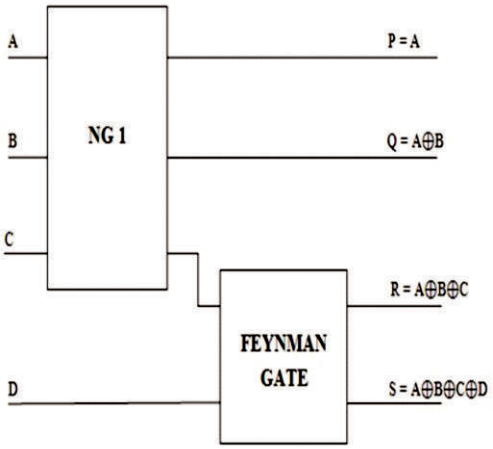


Figure 3. The Proposed Design

the reversible digital circuit shown in Table 2. The proposed design of reversible gray to binary code converters will find applications in quantum computing, nanotechnology, etc.

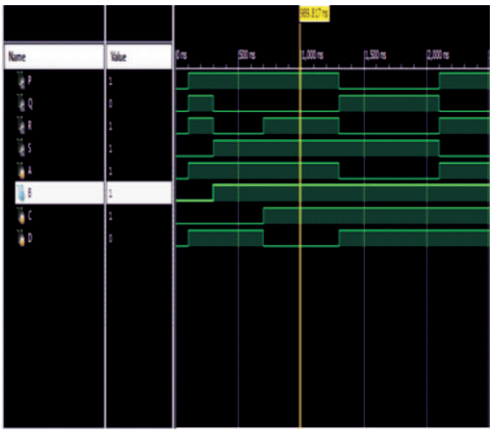


Figure 4. Simulation Result of the Proposed Design

Designs	Gate Count	Constant Inputs	Garbage Outputs	Quantum Cost
Existing Design 1 [6]	5	2	3	5
Existing Design 2 [7]	2	0	0	Not Reported
Proposed Design	2	0	0	3

Table 2. Comparison Table of the Proposed Design with the Existing Designs

References

[1]. Landauer, R. (1961). "Irreversibility and heat generation in the computing process". *IBM Journal of Research and Development,* Vol. 5, No. 3, pp.183-191.

[2]. Bennett, C.H, (1973). "Logical reversibility of Computation". *IBM Journal of Research and Development,* Vol. 17, No. 6, pp.525-532.

[3]. Feynman, R. (1985). "Quantum Mechanical Computers". *Optics News,* Vol. 11, No. 2, pp. 11-20.

[4]. Parhami, B. (2006). "Fault Tolerant Reversible Circuits". *Proc. 40th Asilomar Conf. Signals, Systems, and Computers,* Pacific Grove, CA, pp. 1726-1729.

[5]. Toffoli, T. (1980). *Reversible computing.* Technical Memo MIT/LCS/TM-151, MIT Lab. for Computer Science.

[6]. Saravanan, and M. Suresh Manic, K. (2013). "Energy Efficient Code Converters using Reversible Logic Gates". *International Conference on Green High Performance Computing, IEEE,* pp. 1-6.

[7]. Kotaiah Kamani, Sandeep Koneti, Ujwala Bollampalli, and Sreevanishankara, (2014). "Energy Efficient Reversible logic Design for Code Converters". *ICETET, International Journal of Research and Applications,* Vol. 1, No. 3, pp. 132-136.

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