A NOVEL MULTILEVEL INVERTER WITH MINIMUM SWITCHES

By

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ABSTRACT

This paper presents an unique three phase seven level inverter with reduced number of switches. Multilevel Inverters (MLI) are used in high power and high voltage applications as they are capable of producing multiple levels in output voltage with reduced THD. To reduce THD further, the number of levels in the output voltage has to be increased, which is directly associated with the number of switches required. To accomplish this, the conventional MLI experiences complexity in control, number of required DC sources, size, switching losses and cost of overall system increases. The proposed topology overcomes the aforesaid limitations and compared with the conventional MLI in terms of the number of switches, DC sources, capacitors, fundamental voltage, and THD. The performance is analyzed by using a simulation tool.

Keywords: Multilevel Inverter, THD, Reduced Switches, Level Shifted Carriers, Modulating Techniques.

INTRODUCTION

Based on the circuit configuration, the multilevel inverters are classified as diode clamped, flying capacitor and cascaded [1-3] inverters. Out of which, Cascaded Multilevel Inverter (CMLI) is having more advantages when compared to diode clamped and flying capacitor in terms of the number of switches, control complexity and voltage balancing [3]. Furthermore, clamping diodes and flying capacitors are not required for CMLI With conventional CMLI, the number of levels can be increased by increasing the number of series connected H Bridges. The circuit configuration of three phase CMLI is represented in Figure 1.

This paper presents a novel seven level inverter with reduced number of switches. The numbers of levels are increased by increasing the number of switches instead of adding the H bridge.

The rest of the paper is organized as follows, concept of single phase seven level inverter with reduced number of switches is explained in section 1, the same idea is extended for three phase inverter section 2, different carrier based PWM techniques are discussed in section 3, the simulation results of the proposed and conventional seven level inverters are presented in section 4, finally conclusions are made in the last section .

1. Single Phase Converter

For reducing the number of components, control complexity, cost and size of multilevel inverter used for high voltage and high power applications of a novel single phase five level inverter is explained [5]. The proposed single phase seven level inverter is represented

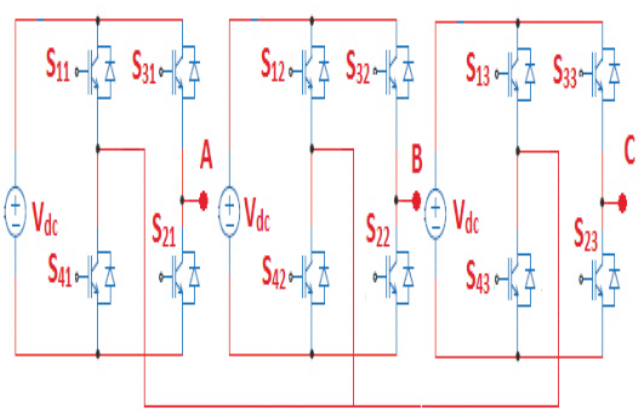


Figure 1. Three Phase CMLI Configuration

in Figure 2. The proposed topology is the cascaded linkage of following parts:

Part I: Level generator which generates the positive stepped waveform across the inverter.

Part II: H Bridge, used for polarity reversal.

The Generalized equation to decide the number of DC sources, and switches required for a proposed MLI is given below:

Number of source required $N_s = (n-1)/2$ (1)

Number of switches = n (2)

Where n is the number of levels in output voltage.

The proposed seven level inverter requires three dc sources of equal magnitude and seven switches. Comparison of different components required for conventional and the proposed MLI's is shown in Table 1.

The proposed seven level inverter is capable of producing seven levels $\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm V_{dc}$ and 0 in the output voltage waveform. The switching sequence t produce these seven levels in the output voltage is shown in Table 2.

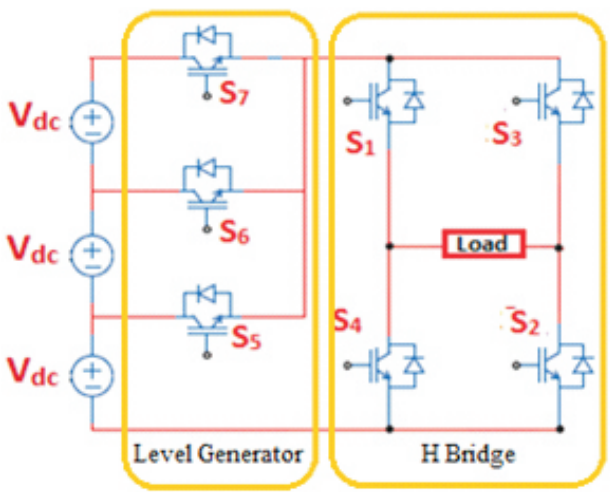


Figure 2. Single Phase Seven Inverter Circuit Configuration

	DCMLI	CCMLI	CHMLI	PMLI
DC Sources	(n-1)	(n-1)	(n-1)/2	(n-1)/2
Main Switch	6*(n-1)	6*(n-1)	6*(n-1)	n
Clamping Diode	3*(n-1) *(n-2)	0	0	0
Clamping Capacitor	0	1.5*(n-1) *(n-2)	0	0

Table 1. Comparison with Conventional MLI

S_1	S_2	S_3	S_4	S_5	S_6	S_7	Output
1	1	0	0	1	0	0	V_{dc}
1	1	0	0	0	1	0	$2V_{dc}$
1	1	0	0	0	0	1	$3V_{dc}$
0	1	1	0	0	0	0	0
1	0	0	1				
0	0	1	1	1	0	0	$-V_{dc}$
0	0	1	1	0	1	0	$-2V_{dc}$
0	0	1	1	0	0	1	$-3V_{dc}$

* 0 = switch turned off, 1 switch turned on

Table 2. Switching Sequence

At any instant only three switches will be conducting. Two switches for polarity reversal and one switch for getting the desired voltage level in the output waveform. Single phase Seven level inverter with nine and ten switches are discussed [6, 7].

2. Proposed Three Phase Seven Level Topology

The concept of proposed single phase seven level inverter can be easily extended to the three phase seven level inverter. The proposed three phase topology is easy to control as the number of switches conducting at any instant is less when compared with conventional topology. Figure 3, represents the circuit configuration of

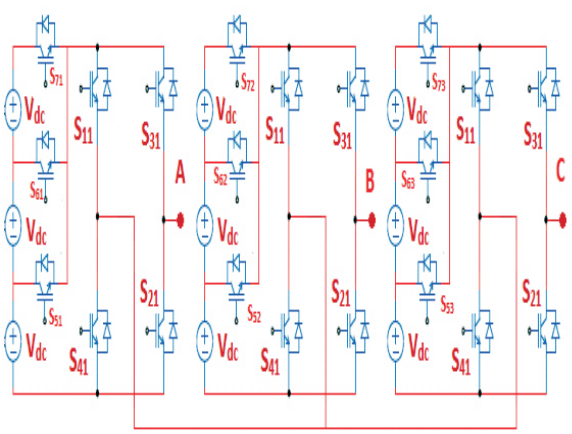


Figure 3. Three Phase Seven Level Inverter

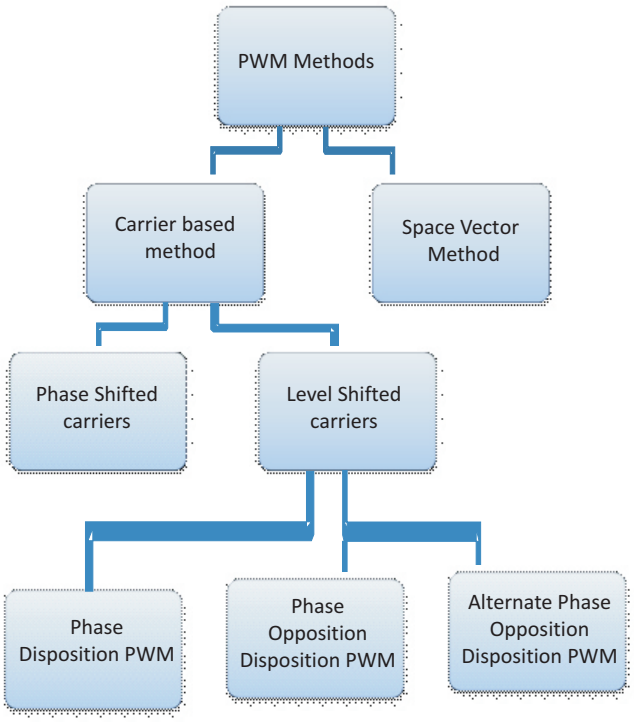


Figure 4. Flow Chart of PWM Methods Classification

the proposed three phase seven level inverter.

3. Carrier Based PWM Techniques

The purpose of PWM is to generate the variable voltage and variable frequency from the fixed DC input. In PWM techniques two signals are used, i.e., carrier and reference signal. When reference is greater than a carrier, ON pulse is generated and OFF pulse is generated when the carrier is greater than the reference [8, 9]. Classification of PWM methods is shown in Figure 4.

With space vector method, the number of switching states

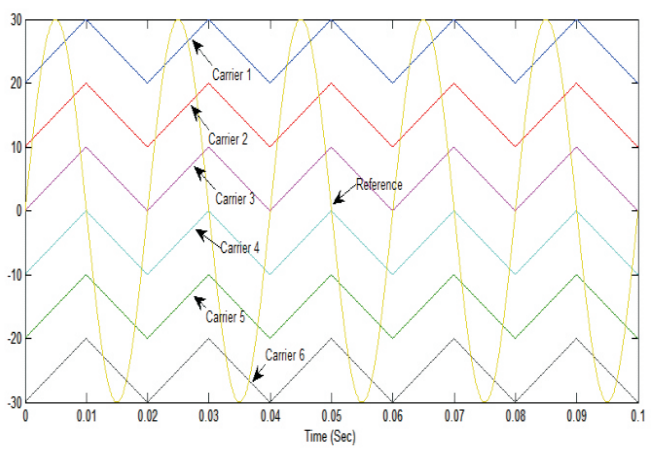


Figure 5. Phase Disposition Carriers

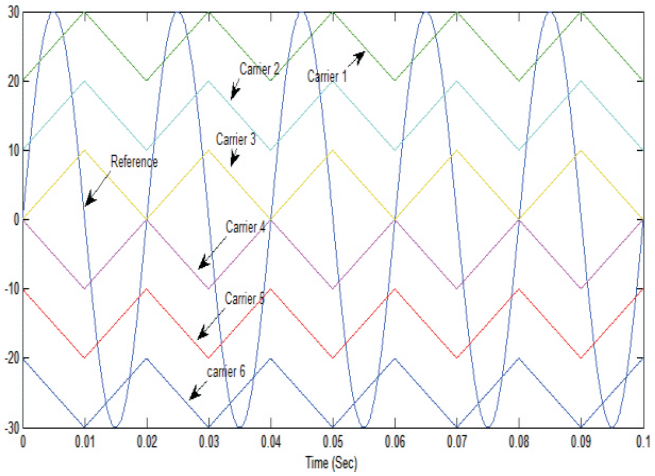


Figure 6. Phase Opposition Disposition Carriers

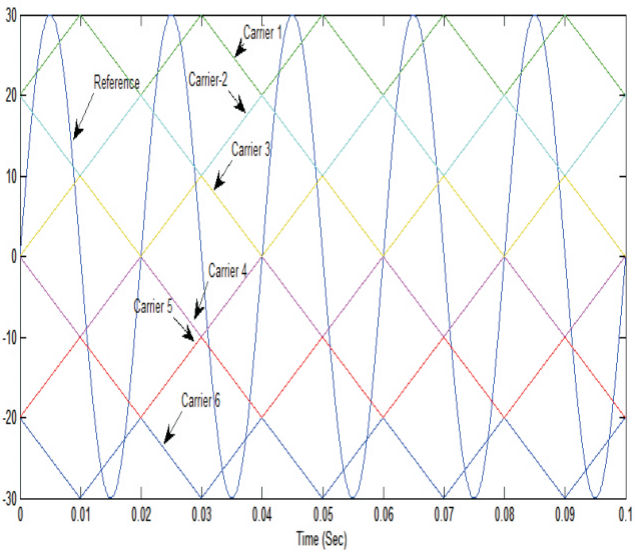


Figure 7. Alternate Phase Opposition Disposition Carriers

is equal to n^3 where n represents the number of levels. It is difficult to identify the sectors, sub sector and switching sequence. The phase shifted carriers generates a lot of harmonics in the output voltage. To overcome the intact drawbacks the level shifted carriers are used.

- *Phase Disposition (PD)* :

  All the carrier waveforms are in phase as shown in Figure 5.

- *Phase Opposition Disposition (POD)* :

  All carrier waveforms above the zero reference are in phase and 180° out of phase with those below zero, which is shown in Figure 6.

- *Alternate Phase Disposition (APOD)* :

  The carrier waveforms are out of phase with its

neighbor carrier by 180° and it is shown in Figure7.

4. Simulation Results

Conventional seven level cascaded and proposed seven level inverters are simulated with level shifted carrier PD, POD and APOD. These inverters are simulated with the following parameters,

Input Voltage = 100V,

Switching Frequency = 10000Hz,

Modulation Index = 1

Resistive Load = 100 Ω.

Figures 8 to 10 show the simulation results for THD and the output line to line voltage for conventional seven level inverter using PD, POD and APOD PWM techniques

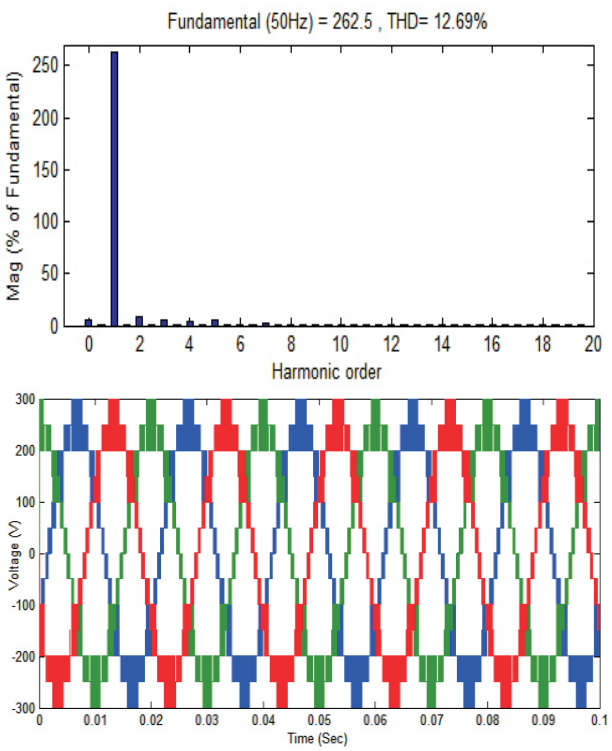
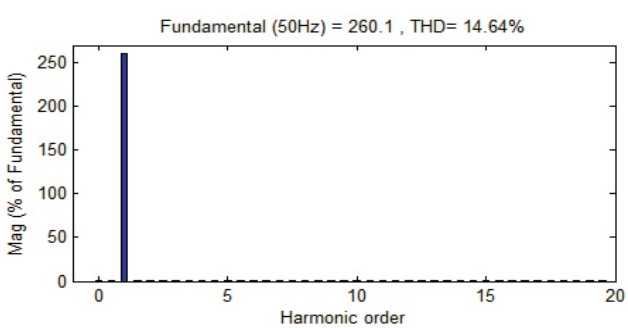


Figure 8. THD and Output Voltage with PD



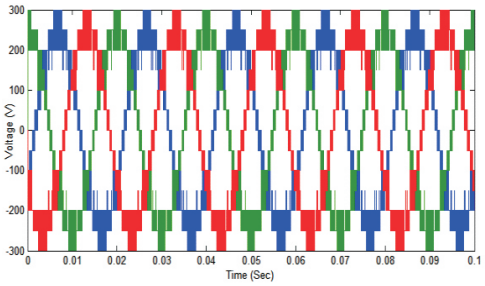
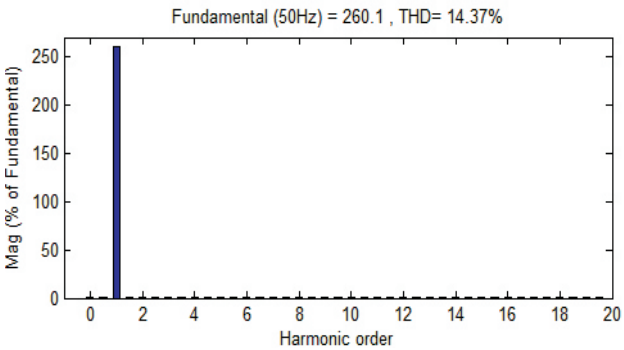


Figure 9. THD and Output Voltage with POD



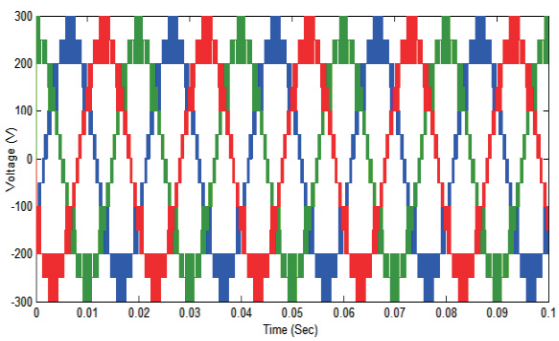


Figure 10. THD and Output Voltage with APOD

respectively.

Figures 11 to 13 show the THD and the output line to line voltage simulation results for proposed seven level inverter using PD, POD and APOD PWM techniques. The comparison results are shown in Table 3.

Conclusion

This paper presents a new three phase seven level inverter with reduced number of switches. The proposed inverter is capable of producing the same fundamental voltage and THD as that of conventional seven level cascaded inverter. The proposed circuit reduces the complexity of control, size and cost of the inverter, as the number of components used in this circuit is equal to a number of levels. The same inverter can be extended to n levels with

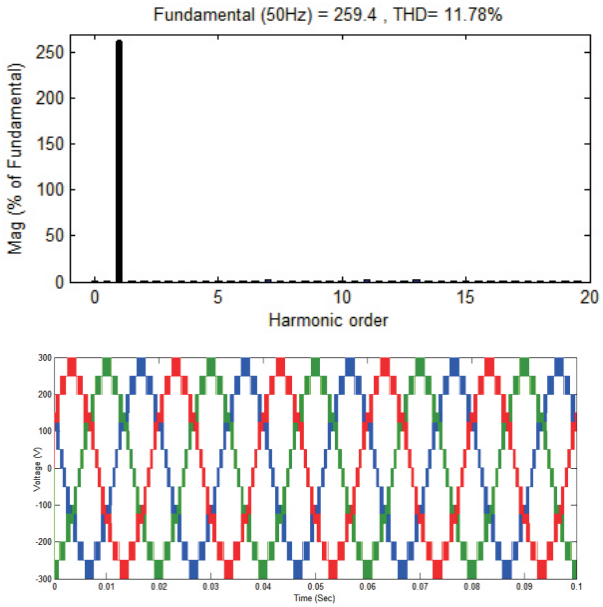


Figure 11. THD and Output Voltage with PD

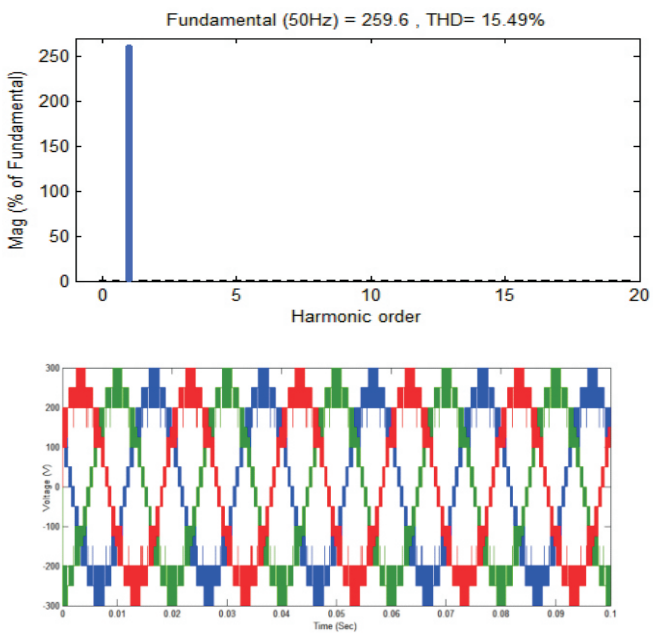
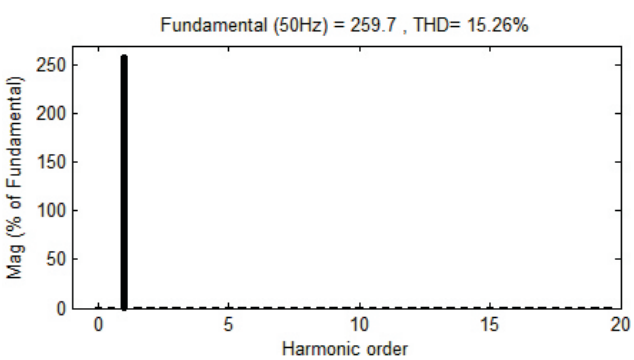


Figure 12. THD and Output Voltage with POD



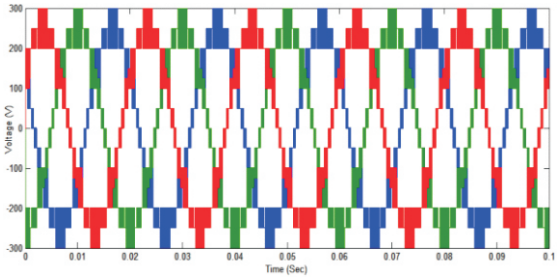


Figure 13. THD and Output Voltage with APOD

Type of carrier	Type of converter	Fundamental Voltage	THD
PD	Conventional	262	12.96
	Proposed	259.4	11.78
POD	Conventional	260.1	14.64
	Proposed	259.6	15.49
APOD	Conventional	260.1	14.37
	Proposed	259.7	15.26

Table 3. Comparison of CMLI's and PMLI

n switches

References

[1]. **Marchesoni. M, (2002).** "Diode-clamped multilevel converters: a practicable way to balance DC-link voltages". *Industrial Electronics, IEEE Transactions,* Vol. 49, No. 4, pp. 752-765.

[2]. **Escalante, Miguel F. Jean-Claude Vannier, and Amir Arzande, (2002).** "Flying capacitor multilevel inverters and DTC motor drive applications." *Industrial Electronics, IEEE Transactions on* , Vol. 49, No. 4 , pp. 809-815.

[3]. **Mariusz Malinowski, K. Gopakumar, Jose Rodriguez and Marcelo A. Perez, (2010).** "A Survey on Cascade Multilevel inverters". *IEEE Trans. Ind. Electron*, Vol. 57, No. 7.

[4]. **Franquelo. L. G., Rodriguez. J., Leon. S., Kouro. J. I., Portillo. R , and Prats. M. A., (2008).** "The age of multilevel converters arrives". *IEEE Ind. Electron. Mag,* Vol. 2, No. 2, pp. 28–39.

[5]. **Nimitha, M. and Ramani T., (2014).**"Simulation & analysis of multilevel inverter with reduced number of switches". *IJEET,* Vol. 5, No .12.

[6]. **Gnana Prakash M., Balamurugan M., and Umashankar S., (2014).** "A New Multilevel Inverter with reduced number of switches". *IJPEDS*, Vol. 5, No. 1.

[7]. S. Nagaraja Rao, D.V. Ashok Kumar. and Ch. Sai Babu, (2013)."New Multilevel Inverter Topology with reduced number of switches using advanced Modulation Strategy".In*: Proceedings of the International Conference on Power, Energy and Control (ICPEC).*

[8]. Manjunatha B. M, Ashok Kumar D. V. and Vijay Kumar, M. (2015). "Advanced Pulse Width Modulation Techniques for Z Source Multi Level Inverter". *World Academy of Science, Engineering and Technology, International Science Index 99, International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering*, Vol. 9, No. 3, pp. 337 - 342.

[9]. Brendan Pete McGrath and Donald Grahame Holmes, (2002). "Multicarrier PWM Strategies for Multilevel Inverters". *IEEE Trans.Ind. Electronics,* Vol. 49, No. 4.

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